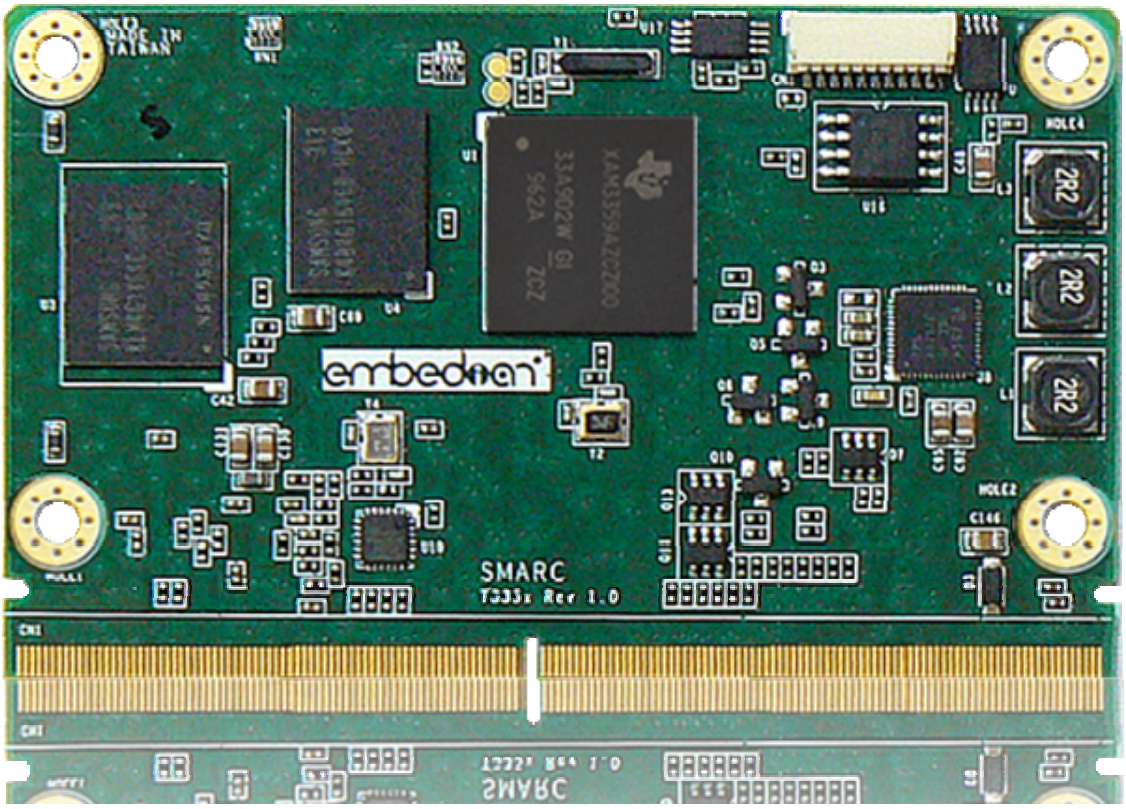
User's Manual

SMARC Computer on Module

TI Sitara AM335x Cortex A8
Parallel LCD 18/24 bits
3 x COM Ports
1 x SDHC
1 x USB Host 2.0, 1 x USB OTG
2 x 10/100Mbps Ethernet
CAN Bus, 2 x SPIs, 3 x I2C

SMARC T335x


embedian
SMARC
T335x Rev 1.0

Revision History

Revision	Date	Changes from Previous Revision
1.0	2013/4/16	Initial Release
1.01	2013/5/06	1. Correct Boot Configuration 2. Correct Debugging Port from SER1 to SER3 3. Add module EEPROM Format Information
1.02		1. Correct the rtc-s35390a i2c address from 0x34 to 0x30

USER INFORMATION

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Using this Manual

This guide provides information about the Embedian SMARC (formerly ULP-COM) T335X for TI AM335x embedded SMARC core module family.

Conventions used in this guide

This table describes the typographic conventions used in this guide:

This Convention	Is used for
Italic type	Emphasis, new terms, variables, and document titles.
`monospaced type`	Filenames, pathnames, and code examples.

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Additional Resources

Please also refer to the most recent TI AM335x processor reference manual

and related documentation for additional information.

Introduction

This Chapter gives background information on the SMARC T335X
Section include：

- Features and Functionality
- Module Variant
- Block diagram
- Software Support / Hardware Abstraction
- Module Variant
- Document and Standard References

Chapter 1 Introduction

The SMARC® (**S**mart **M**obility **ARC**hitecture, formerly ULP-COM, **U**ltra **L**ow **P**ower – **C**omputer **o**n **M**odule) T335x is a versatile small form factor Computer-On-Module that requires low power and provides high performance at low cost. The module connector has 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector (this connector is sometimes identified as an 321 pin connector, but 7 pins are lost to the key).
Featuring TI's AM335x System-on-Chip, Embedian's SMARC T335X offers Parallel LCD, two 10/100Mbps Ethernet, SDHC, USB 2.0, USB OTG, three UARTs support and many peripheral interfaces in a cost effective, low power, miniature package. Embedian's SMARC T335X thin and robust design makes it an ideal building block for reliable system design.

The module is the ideal choice for a broad range of target markets including

- HVAC Building and Control Systems
- Fire Alarms
- Smart Grid and Smart Metering
- E-Bike
- HMI/ In-Home Display
- Smart Toll Systems
- Connected Vending Machines
- Fiscal Printer/ Weighing Scales/ Currency Counter
- And more

Complete and cost-efficient Embedian evaluation kits for Ubuntu 12.04, Android ICS and Microsoft Windows Embedded Compact 7 allow immediate and professional embedded product development with dramatically reduced design risk and time-to-market.

1.1 Features and Functionality

The SMARC T335X module is based on the AM335x processor from Texas Instruments. This processor offers a high number of interfaces. Most of these interfaces are multiplexed and are not available simultaneously. The module has the following features:

- SMARC (ULP-COM) compliant in an 82mm x 50mm form factor.
- Processor: TI Sitara AM335x ARM Cortex-A8 up to 1GHz
- Memory: Onboard 4GB eMMC Flash and 4MB SPI NOR Flash
- Onboard 512MB DDR3 (606Mhz)

- Networking: 2 x 10/100 Mbps Ethernet
- Display: Parallel LCD 18-bit/24-bit
- Expansion: 1 x SDHC/SDIO, 1 x USB 2.0 Host
- USB: 1 x USB 2.0 Host, 1 x USB 2.0 OTG
- A single 4KB EEPROM is provided on I2C0 that holds the board information. This information includes board name, serial number, and revision information.
- Additional Interface:
  - 3 x UARTs
  - 2 x SPI
  - 3 x I2C
  - 1 x I2S
  - 1 x CAN Bus
  - 1 x PWM
  - 12 x GPIOs
  - 4 x ADCs
  - WDT
- SW Support: Linux (Ubuntu 12.04), Android ICS, Windows Embedded Compact 7
- Power Consumption: 1.5 Watts Typical
- Thermal:
  - Normal Temperature: 0^{o}C ~ 60^{o}C
  - Industrial Temperature: -40^{o} ~85^{o}C
- Power Supply
- 3V to 5.25V (single 5V is recommended in non-battery operation)
- 3.3V module IO support

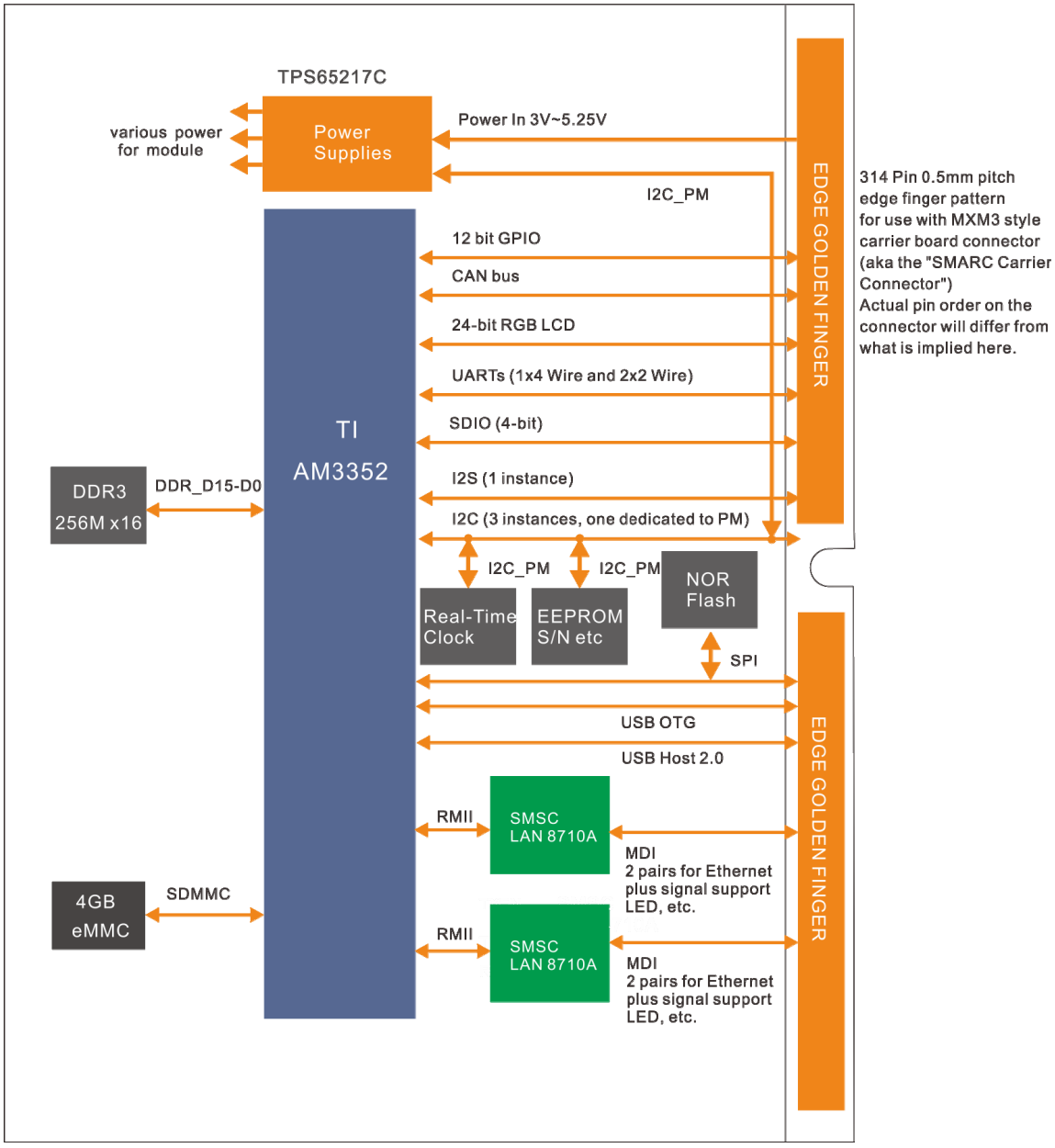
1.2 Module Variant

The SMARC T335X module is available with various options based on processors in this family from Texas Instruments. For example, if people would like to use Sitara AM3354 from Texas Instruments, you can order SMARC T3354.

1.3 Block Diagram

The following diagram illustrates the system organization of the SMARC T335X. Arrows indicate direction of control and not necessarily signal flow.

Figure 1: SMARC T335X Block Diagram



Details for this diagram will be explained in the following chapters.

1.4 Software Support / Hardware Abstraction

The Embedian SMARC T335X Module is supported by Embedian BSPs (Board Support Package). The first SMARC T335X BSP targets Linux (Ubuntu 12.04 LTS) and Android support. BSPs for other operating systems are planned. Check with your Embedian contact for the latest BSPs.
This manual goes into a lot of detail on I/O particulars – information is provided on exactly how the various SMARC edge fingers tie into the TI SoC and to other Module hardware. This is provided for reference and context. Almost all of the I/O particulars are covered and abstracted in the BSP and it should generally not be necessary for users to deal with I/O at the register level.

1.5 Document and Standard References

1.5.1. External Industry Standard Documents

- ***eMMC (Embedded Multi-Media Card)*** the eMMC electrical standard is defined by JEDEC JESD84-B45 and the mechanical standard by JESD84-C44 (www.jedec.org).
- ***The I2C Specification,*** Version 2.1, January 2000, Philips Semiconductor (now NXP) (www.nxp.com).
- ***I2S Bus Specification,*** Feb. 1986 and Revised June 5, 1996, Philips Semiconductor (now NXP) (www.nxp.com).
- ***JTAG (Joint Test Action Group*** defined by IEEE 1149.1-2001 - IEEE Standard Test Access Port and Boundary Scan Architecture (www.ieee.org).
- ***MXM3 Graphics Module Mobile PCI Express Module Electromechanical Specification,*** Version 3.0, Revision 1.1, © 2009 NVIDIA Corporation (www.mxm-sig.org).
- ***PICMG® EEEP Embedded EEPROM Specification,*** Rev. 1.0, August 2010 (www.picmg.org).
- ***SD Specifications Part 1 Physical Layer Simplified Specification,*** Version 3.01, May 18, 2010, © 2010 SD Group and SD Card Association (Secure Digital) (www.sdcard.org).
- ***SPI Bus –*** “Serial Peripheral Interface” - de-facto serial interface standard defined by Motorola. A good description may be found on Wikipedia (http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus).
- ***USB Specifications*** (www.usb.org).

1.5.2. SGET Documents

- ***SMARC_Hardware_Specification_V1p0***, version 1.0, December 20, 2012.

1.5.3. Embedian Documents

The following documents are listed for reference. The Module schematic is not usually available outside of Embedian, without special permission. The other schematics may be available, under NDA or otherwise. Contact your Embedian representative for more information. The SMARC T335x Evaluation Carrier Board Schematic is particularly useful as an example of the implementation of various interfaces on a Carrier board.

- ***SMARC_T335x Evaluation Carrier Board Schematic***, PDF and OrCAD format
- ***SMARC_T335x Evaluation Carrier Board User's Manual***
- ***SMARC_T335x Carrier Board Hardware Design Guide***
- ***SMARC_T335x Carrier Board Hardware Layout Guide***
- ***SMARC_T335x User's Manual***
- ***SMARC_T335X Schematic Checklist***

1.5.4. TI Documents

- ***AM335x ARM Cortex-A8 Microprocessors (MPUs),*** April 15 2013 (rev. F)
- ***AM335x Schematic Checklist***, Oct 31 2011
- ***AM335x ARM Cortex-A8 Microprocessors (MPUs) Technical References Manual***, April 15 2013 (rev. H)
- ***AM335x Power Consumption Summary***, Oct 31 2011

1.5.5. TI Development Tools

- ***Pin Mux Utility for ARM® Microprocessors***
- ***Power Estimation Tool (PET)***

1.5.6. TI Software Documents

- ***LINUXEZSDK-AM335x***
- ***ANDROIDDEVKIT-JB-AM335x***

1.5.7. Embedian Software Documents

- ***Embedian Linux BSP for SMARC T335X Module***
- ***Embedian Android BSP for SMARC T335X Module***
- ***Embedian Linux BSP User's Guide***
- ***Embedian Android BSP User's Guide***

1.5.8. TI Design Network

- ***Beaglebone***
- ***Adeneo Embedded (Windows Embedded Compact 7)***
- ***Nucleus***
- ***QNX***

Specifications

This Chapter provides SMARC T335X specifications.
Section include：

- SMARC T335X General Functions
- SMARC T335X Debug
- Mechanical Specifications
- Electrical Specification
- Environment Specification

Chapter 2 Specifications

2.1 SMARC T335X General Functions

2.1.1. SMARC T335X Feature Set

This section lists the complete feature set supported by the SMARC T335X module.

SMARC Feature Specification	SMARC Specification Maximum Number Possible	SMARC T335X Feature Support	SMARC T335X Feature Support Instances
LVDS Display Support	1	No (transmitter on carrier)	0
Parallel LCD Support	1	Yes	1 (18/24 bits)
HDMI Display Support	1	No	0
CSI Camera Support (Dual and Quad lanes)	2	No	0
Parallel Camera Support	2	No	0
USB Interface	3	Yes	2
PCIe Interface	3	No	0
SATA Interface	1	No	0
GbE Interface	1	10/100Mbps	1
SDIO Interface	1	Yes	1
SDMMC Interface	1	No (4GB eMMC on module)	0
SPI Interface	2	Yes	2
I2S Interface	3	Yes	1
I2C Interface	5	Yes	3
Serial	4	Yes	3
CAN	2	Yes	1

SMARC Feature Specification	SMARC Specification Maximum Number Possible	SMARC T335X Feature Support	SMARC T335X Feature Support Instances
AFB		Yes	2nd LAN and resistive touch
I/O Voltage (1.8V) Level Support		No	
I/O Voltage (3.3V) Level Support		Yes	

2.1.2. Form Factor

The SMARC T335X module complies with the SMARC General Specification module size requirements in an 82mm x 50mm form factor.

2.1.3. CPU

The SMARC T335X implements TI's AM335x ARM processor.

- Up to 1GHz ARM Cortex-A8 Microprocessor
- 1 Cache 32 KB Instruction cache (I-Cache) and 32 KB Data cache (D-Cache) with Single-Error Detection (parity)
- 256KB of L2 Cache with Error Correcting - Emulation and Debug Code (ECC)
- 176KB of On-Chip Boot ROM
- 64KB of Dedicated RAM
- SGX530 graphic engine
- Programmable Real-Time Unit and Industrial - Dedicated Input Pin (EXT_WAKEUP) for Communication Subsystem (PRU-ICSS)
    - Supports protocols such as EtherCAT®, PROFIBUS, PROFINET, EtherNet/IP™, and more.
- 15mm x 15mm (ZCZ) package size
- Optional industrial temperature rage -40°C ~ 85°C

Note: SGX530 graphics support for AM3354 and AM3358 processor (pin-to-pin).

2.1.4. Module Memory

The SMARC T335X module supports 512MB DDR3 memory. Other variations would include alternative eMMC options, including possibly no on-Module eMMC. Check with your Embedian contact or on the Embedian web site for updated information.

2.1.5. Onboard Storage

The SMARC T335X module supports a 4GB eMMC flash memory device, 4MB SPI NOR flash and a 32Kb I2C serial EEPROM on the Module I2C_PM (I2C0) bus. The device used is an On Semiconductor 24C32 equivalent. The Module serial EEPROM is intended to retain Module parameter information, including a module serial number. The Module serial EEPROM data structure conforms to the PICMG® EEEP Embedded EEPROM Specification.). The onboard 4MB SPI NOR flash that can be used as SPI boot media or for users to store secure data.

2.1.6. Clocks

A 32.768 KHz clock is required for the TM335x CPU RTC (Real Time Clock) and I2C RTC slave device.
The TI AM335x CPU is provided with a 24 MHz clock using a crystal in normal oscillation mode (On-chip Oscillator).
The SMSC LAN8720A PHY is provided with a 25 Mhz clock using a crystal in normal oscillation mode.

2.1.7. Parallel LCD Interface

The TI AM335x parallel 24 bit LCD interface is brought to the Module edge connector. The interface runs at the 3.3V Module I/O voltage. This voltage swing may be used directly with 3.3V capable Carrier Board LVDS transmitters, such as the TI SN75LVDS83B. The 3.3V signaling is suitable for direct connection to a parallel flat panel in most cases. Generally speaking, larger parallel LCD panels are likely to use 3.3V or 5V signaling. If LCD panels use 5V signaling, a set of voltage translators / buffers would be needed on the Carrier.

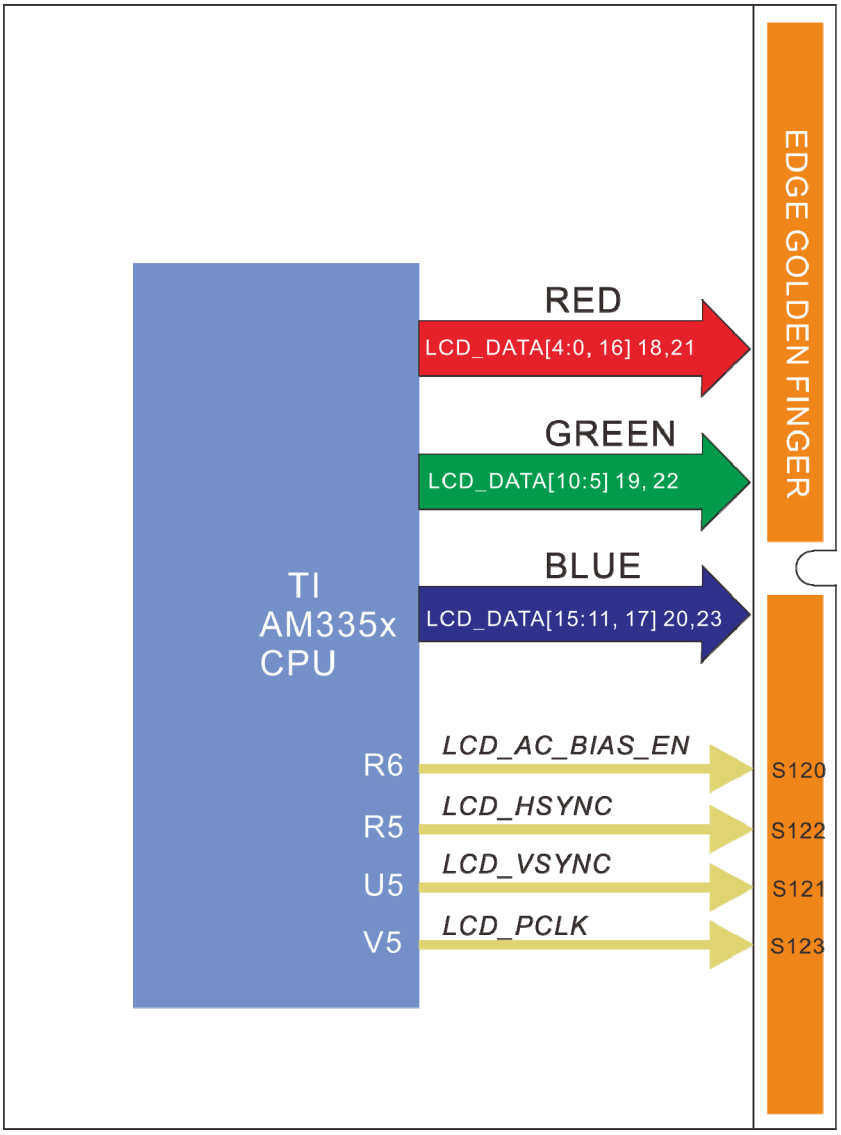


Figure 2: SMARC T335X Block Diagram

The mapping of the TI AM335x parallel LCD pins to the SMARC edge connector is shown in the table below. Note that the TI Sitara AM335x pin names and the SMARC pin names have different assumptions about color mappings, which can make things confusing. Basically, TI Sitara AM335x processor maps the 18 bits or R, G, B for 6 bit color depth to *LCD_DATA[17:0]*. For Sitara AM335x, the extra bits used for a 24 bit color implementation come out on TI *LCD_DATA[23:18]*. Since 18-bit configuration and 24-bit configuration use the same MSB signals, we can say 18-bit configuration is higher bits subset 24-bit configuration from the hardware point of view. The SMARC has a different convention: Red is *LCD_D[23:16]*; Blue is *LCD_D[15:8]* and Green is *LCD_D[7:0]*. For 24 bit implementations, all bits are used. For 18 bit implementations, in SMARC, the least significant bits (Red *LCD_D[17:16]*, Green *LCD_D[9:8]*, Blue *LCD_D[1:0]*) are dropped.

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names (Carrier Board)	Color	24-bit Color Map
Ball	Mode	Pin Name	Pin#	Pin Name			
T1	Mode0	LCD_DATA4	S118	LCD_D23 (MSB)	LCD_D23	RED	R7
R4	Mode0	LCD_DATA3	S117	LCD_D22	LCD_D22		R6
R3	Mode0	LCD_DATA2	S116	LCD_D21	LCD_D21		R5
R2	Mode0	LCD_DATA1	S115	LCD_D20	LCD_D20		R4
R1	Mode0	LCD_DATA0	S114	LCD_D19	LCD_D19		R3
U13	Mode1	LCD_DATA16	S113	LCD_D18	LCD_D18		R2
R12	Mode1	LCD_DATA18	S112	LCD_D17	LCD_D17		R1
T11	Mode1	LCD_DATA21	S111	LCD_D16 (LSB)	LCD_D16		R0
U3	Mode0	LCD_DATA10	S109	LCD_D15 (MSB)	LCD_D15	GREEN	G7
U2	Mode0	LCD_DATA9	S108	LCD_D14	LCD_D14		G6
U1	Mode0	LCD_DATA8	S107	LCD_D13	LCD_D13		G5
T4	Mode0	LCD_DATA7	S106	LCD_D12	LCD_D12		G4
T3	Mode0	LCD_DATA6	S105	LCD_D11	LCD_D11		G3
T2	Mode0	LCD_DATA5	S104	LCD_D10	LCD_D10		G2
T12	Mode1	LCD_DATA19	S103	LCD_D9	LCD_D9		G1
T10	Mode1	LCD_DATA22	S102	LCD_D8 (LSB)	LCD_D8		G0
T5	Mode0	LCD_DATA15	S100	LCD_D7 (MSB)	LCD_D7	BLUE	B7
V4	Mode0	LCD_DATA14	S99	LCD_D6	LCD_D6		B6
V3	Mode0	LCD_DATA13	S98	LCD_D5	LCD_D5		B5
V2	Mode0	LCD_DATA12	S97	LCD_D4	LCD_D4		B4
U4	Mode0	LCD_DATA11	S96	LCD_D3	LCD_D3		B3
V13	Mode0	LCD_DATA17	S95	LCD_D2	LCD_D2		B2
U12	Mode1	LCD_DATA20	S94	LCD_D1	LCD_D1		B1
U10	Mode1	LCD_DATA23	S93	LCD_D0 (LSB)	LCD_D0		B0

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Color	24-bit Color Map
Ball	Mode	Pin Name	Pin#	Pin Name			
V5	Mode0	LCD_PCLK	S123	LCD_PCK	LCD_PCLK		
R6	Mode0	LCD_AC_BIAS_EN	S120	LCD_DE	LCD_DE		
R5	Mode0	LCD_HSYNC	S122	LCD_HS	LCD_HSYNC		
U5	Mode0	LCD_VSYNC	S121	LCD_VS	LCD_VSYNC		

To use displays which require fewer bits (e.g. 18 or 16 bit displays), simply do not connect the bottom n LSBs for each color, where n is the number of signals that are not required for a specific color. For instance, to connect an 18 bit display, R0, R1, G0, G1, B0 and B1 will remain unused, and R2, G2 and B2 become the LSBs for this configuration.

2.1.8. USB Interface

The Embedian SMARC T335X module supports two USB ports (*USB 0:1*). Per the SMARC specification, the module supports a USB "On-The-Go" (OTG) port capable of functioning either as a client or host device, on the SMARC USB0 port. The SMARC T335X module also supports one additional USB2.0 host ports, on SMARC USB1.
USB interface signals are exposed on the SMARC T335X edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
USB0 Port (OTG)						
N17	Mode0	USB0_DP	P60	USB0+	USB0+	USB0 port data pair
N18	Mode0	USB0_DM	P61	USB0-	USB0-	
F16	Mode0	USB0DRVVBUS	P62	USB0_EN_OC#	USB0_EN_OC#	USB Port0 power enable/over current indication signal
P15	Mode0	USB0_VBUS	P63	USB0_VBUS_DET	5V tolerant	USB host power detection, when this port is used as a device.
P16	Mode0	USB0_ID	P64	USB0_OTG_ID	USB0_ID	USB OTG ID input, active high
USB1 Port (Host 2.0)						
R18	Mdde0	USB1_DP	P65	USB1+	USB1_DP	USB1 port data pair
R17	Mode0	USB1_DM	P66	USB1-	USB1_DM	
F15	Mode0	USB1DRVVBUS	P67	USB1_EN_OC#	USB1_EN_OC#	USB Port0 power enable/over current indication signal

The SMARC Hardware specification defines *USBx_EN_OC#* (where x is 0 or 1 for use with USB0 or USB1) pins as multifunction pins to use for power enable of USBx ports, as well as for over current indication. The SMARC T335X complies with this definition. These nets are provided with a 10k pull up resistors on the Module.

The SMARC T335X Module USB power enable and over current indication logic implementation is shown in the following block diagram. There are 10K pull-up resistors on the Module on the SMARC *USBx_EN_OC#* lines. Outputs driving the *USBx_EN_OC#* lines are open-drain. The Carrier board USB power switch, if present, is enabled by virtue of the 10K Module pull-up to 3.3V.

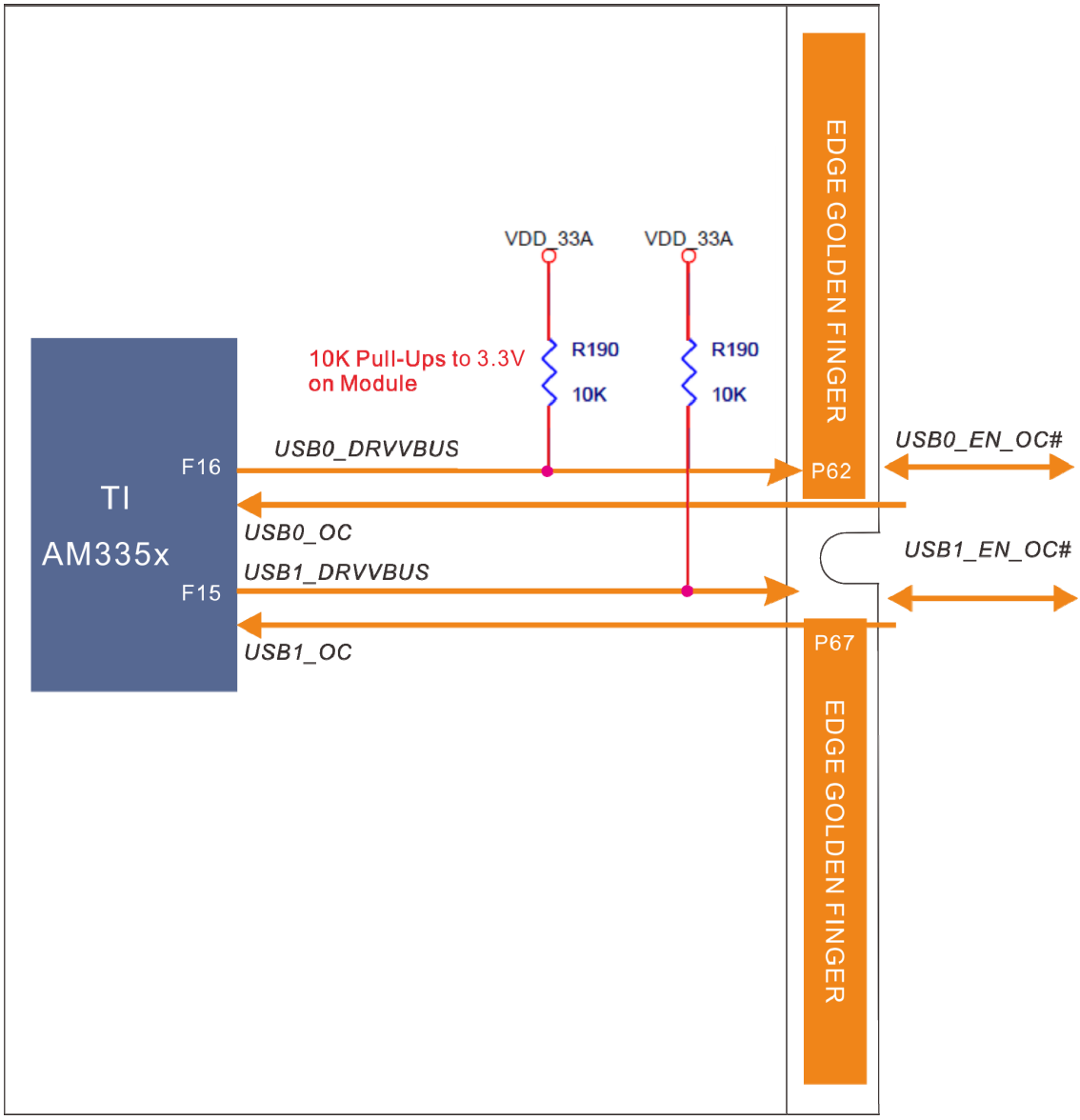


Figure 3. External USB Port Power Distribution Logic Implementation

Power distribution for external USB plug-in peripherals (USB memory sticks, cameras, keyboards, mice, etc.) is typically handled by USB power switches such as the Texas Instruments TPS2052B, Micrel MIC2026-1 or similar devices on the Carrier board.

The Enable pin on the Carrier board USB power switch must be active – high and the Over-Current pin (*OC#*) must be open drain, active low (these are commonly available). No pull-up is required on the USB power switch Enable or *OC#* line; they are tied together on the Carrier and fed to the Module *USBx_EN_OC#* pin. The pull-up is on the Module.

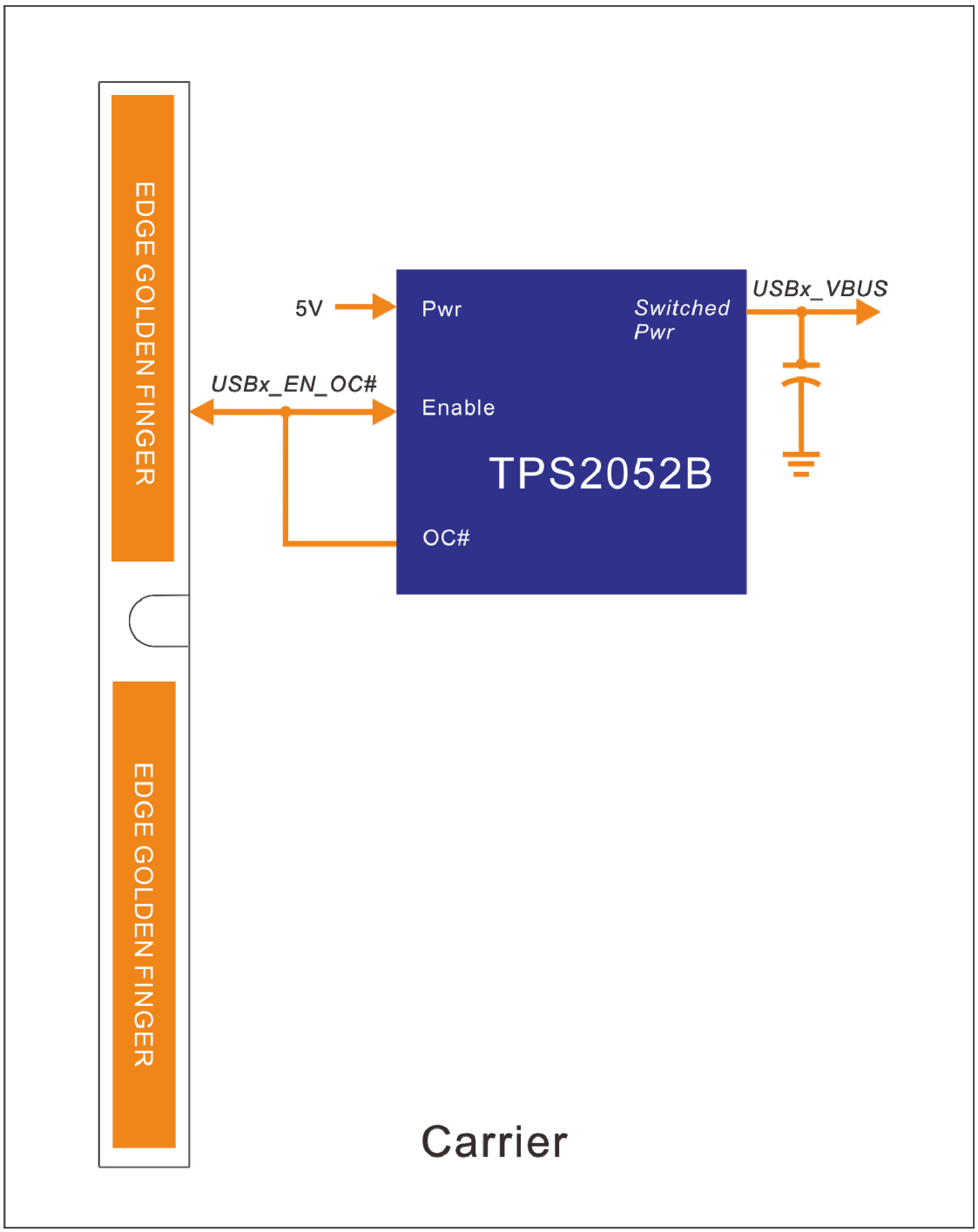


Figure 4. USB Power Distribution Implementation on Carrier

2.1.9. Fast Ethernet Controller (10/100Mbps) Interface

Sitara AM335x CPU offers a high number of interfaces include, but most of these interfaces are multiplexed and are not available simultaneously. This processor can be configured as one Gigabit LAN (MAC) or two 10/100Mpbs LAN (MAC). The SMARC T335X module supports two fast Ethernet (10/100Mbps) interfaces. Two fast Ethernet controller interfaces are

accomplished by using the low-power SMSC LAN8720A physical layer (PHY) transceiver with variable I/O voltage that is compliant with the IEEE 802.3-2005 standards. The LAN8720A supports communication with an Ethernet MAC via a standard RMII interface. This is diagrammed below.

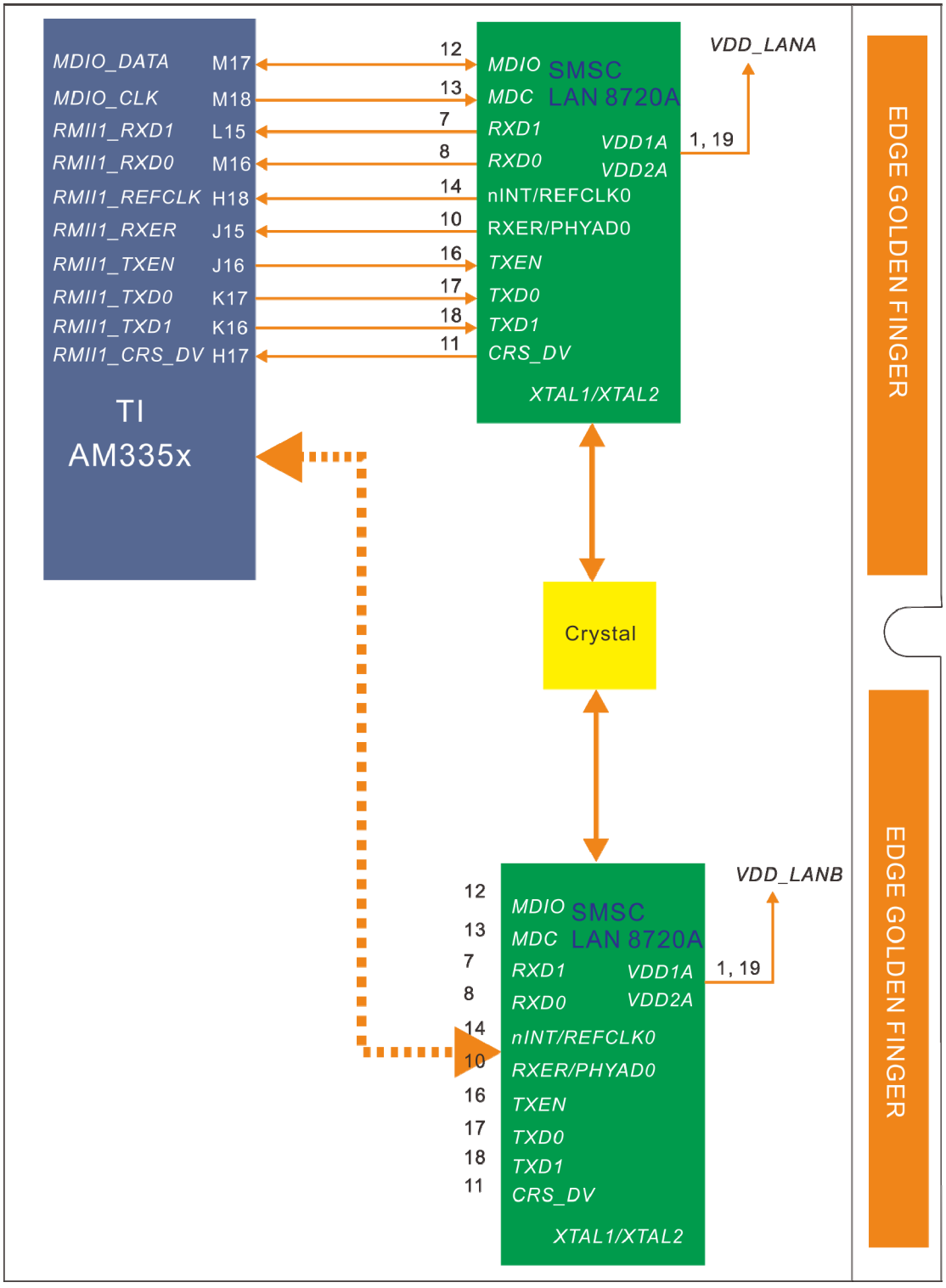


Figure 5: Fast Ethernet Connection from Sitara AM335x to SMSC LAN8720A

Sitara AM335x and SMSC LAN8720A implementation is shown in the following table:

TI AM335x CPU			SMSC LAN8720A		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
LAN1						
M17	Mode0	MDIO_DATA	12	MDIO	MDIO_DATA	Serial Management Interface data input/output
M18	Mode0	MDIO_CLK	13	MDC	MDIO_CLK	Serial Management Interface clock
L15	Mode1	RMII1_RXD1	7	RXD1	RMII1_RXD1	Bit 1 of the 2 data bits that are sent by the transceiver on the receive path.
M16	Mode1	RMII1_RXD0	8	RXD0	RMII1_RXD0	Bit 0 of the 2 data bits that are sent by the transceiver on the receive path.
H18	Mode0	RMII1_REFCLK	14	nINT/REFCLKO	RMII1_RXCLK	Reference clock
J15	Mode1	RMII1_RXER	10	RXER/PHYAD0	RMII1_RXER	This signal is asserted to indicate that an error was detected somewhere in the frame presently being transferred from the transceiver.
J16	Mode1	RMII1_TXEN	16	TXEN	RMII1_TXEN	Indicates that valid transmission data is present on TXD[1:0].
K17	Mode1	RMII1_TXD0	17	TXD0	RMII1_TXD0	The MAC transmits data to the transceiver using this signal.
K16	Mode1	RMII1_TXD1	18	TXD1	RMII1_TXD1	The MAC transmits data to the transceiver using this signal.

TI AM335x CPU			SMSC LAN8720A		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
LAN1						
H17	Mode1	RMII1_CRS_DV	11	CRS_DV	RMII1_CRS_DV	This signal is asserted to indicate the receive medium is non-idle. When a 10BASE-T packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received.
LAN2						
M17	Mode0	MDIO_DATA	12	MDIO	MDIO_DATA	Serial Management Interface data input/output
M18	Mode0	MDIO_CLK	13	MDC	MDIO_CLK	Serial Management Interface clock
T16	Mode3	RMII2_RXD1	7	RXD1	RMII2_RXD1	Bit 1 of the 2 data bits that are sent by the transceiver on the receive path.
V17	Mode3	RMII2_RXD0	8	RXD0	RMII2_RXD0	Bit 0 of the 2 data bits that are sent by the transceiver on the receive path.
H16	Mode1	RMII2_REFCLK	14	nINT/REFCLKO	RMII2_RXCLK	Reference clock
U17	Mode3	RMII2_RXER	10	RXER/PHYAD0	RMII2_RXER	This signal is asserted to indicate that an error was detected somewhere in the frame presently being transferred from the transceiver.
R13	Mode3	RMII2_TXEN	16	TXEN	RMII2_TXEN	Indicates that valid transmission data is present on TXD[1:0].

TI AM335x CPU			SMSC LAN8720A		Net Names	Note
Ball	Mode	Pin Name	Pin #	Pin Name		
LAN2						
V15	Mode3	RMII2_TXD0	17	TXD0	RMII2_TXD0	The MAC transmits data to the transceiver using this signal.
R14	Mode3	RMII2_TXD1	18	TXD1	RMII2_TXD1	The MAC transmits data to the transceiver using this signal.
T17	Mode3	RMII2_CRS_DV	11	CRS_DV	RMII2_CRS_DV	This signal is asserted to indicate the receive medium is non-idle. When a 10BASE-T packet is received, CRS_DV is asserted, but RXD[1:0] is held low until the SFD byte (10101011) is received.

One fast Ethernet port is exposed to GbE port in SMARC golden finger edge connector, the other one is exposed to AFB (Alternative Function Block) pins that has second GbE port definition in SMARC specification. The pin-outs of fast Ethernet (10/100Mbps) are a subset of GbE that defines in SMARC spec. The path from LAN8720A to the golden finger edge connector is show in the following figure.

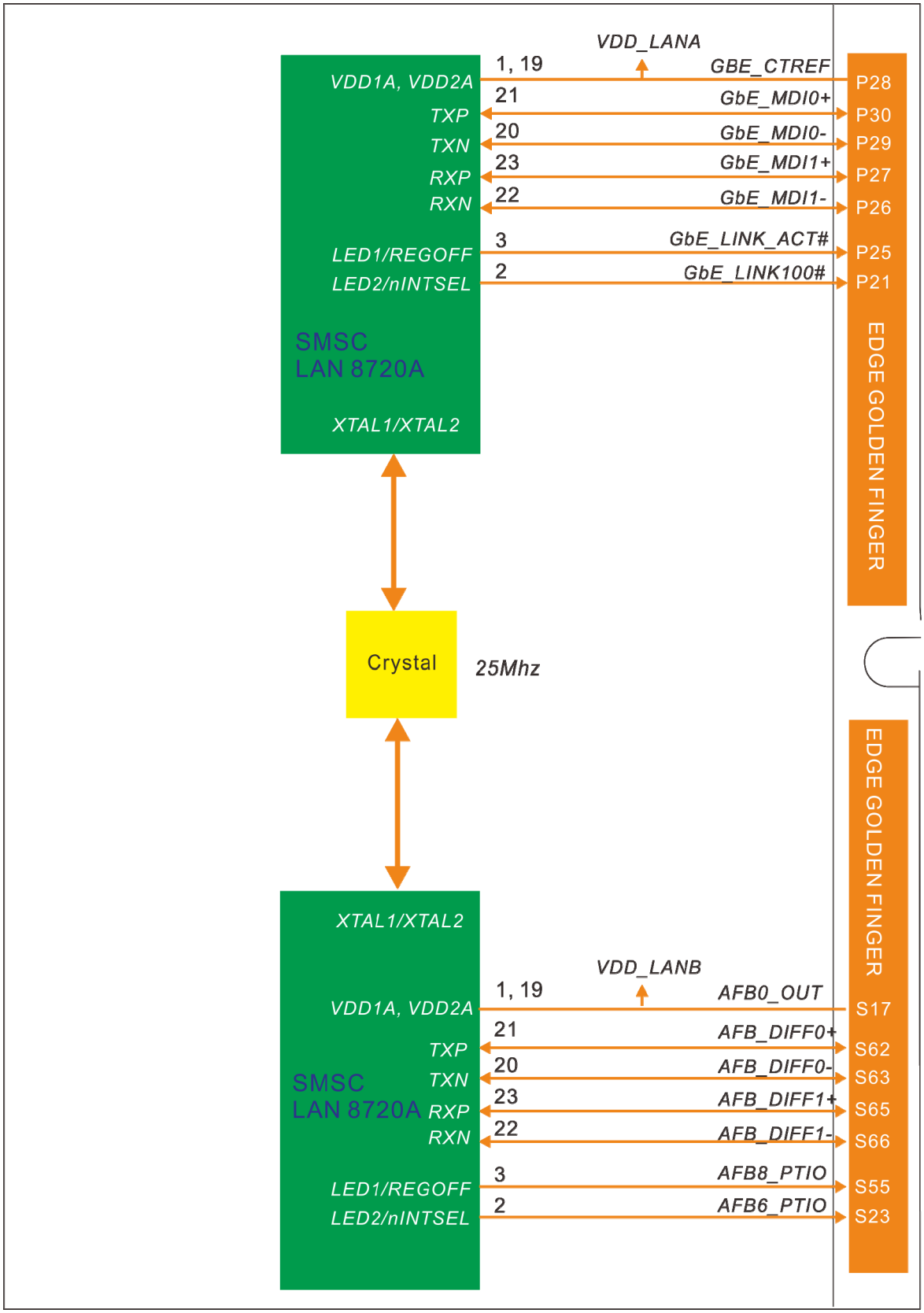


Figure 6: Fast Ethernet Connection from SMSC LAN8720A to golden finger edge connector

SMSC LAN8720A		Golden Finger Edge Connector		Net Names	Note
Pin	Pin Name	Pin#	Pin Name		
LAN1					
21	TXP	P30	GbE_MDI0+	GBE_MDI0+	Differential Transmit/Receive Positive Channel 0
20	TXN	P29	GbE_MDI0-	GBE_MDI0-	Differential Transmit/Receive Negative Channel 0
1,19	VDD1A, VDD2A	P28	GbE_CTREF	GBE_CTREF	Center tap reference voltage
23	RXP	P27	GbE_MDI1+	GBE_MDI1+	Differential Transmit/Receive Positive Channel 1
22	RXN	P26	GbE_MDI1-	GBE_MDI1-	Differential Transmit/Receive Negative Channel 1
3	LED1/REGOFF	P25	GbE_LINK_ACT#	GBE_LINK_ACT#	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
2	LED2/nINTSEL	P21	GbE_LINK100#	GBE_LINK100#	Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current

SMSC LAN8720A		Golden Finger Edge Connector		Net Names	Note
Pin	Pin Name	Pin#	Pin Name		
LAN2					
21	TXP	S62	AFB_DIFF0+	GBE1_MDI0+	Differential Transmit/Receive Positive Channel 0
20	TXN	S63	AFB_DIFF0-	GBE1_MDI0-	Differential Transmit/Receive Negative Channel 0
1,19	VDD1A, VDD2A	S17	AFB0_OUT	GBE1_CTREF	Center tap reference voltage
23	RXP	S65	AFB_DIFF1+	GBE1_MDI1+	Differential Transmit/Receive Positive Channel 1
22	RXN	S66	AFB_DIFF1-	GBE1_MDI1-	Differential Transmit/Receive Negative Channel 1
3	LED1/REGOFF	S55	AFB8_PTIO	GBE1_LINK_ACK#	Link / Activity Indication LED Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity Could be able to sink 24mA or more Carrier LED current
2	LED2/nINTSEL	S23	AFB6_PTIO	GBE1_LINK100#	Link Speed Indication LED for 100Mbps Could be able to sink 24mA or more Carrier LED current

Caution: Due to SMARC T335x support Fast Ethernet instead of Gigabit LAN, GBE_MDI2 (+ and -) and GBE_MDI3 (+ and -) are not connected to the golden finger connector.

2.1.9.1. Termination on Module

The SMSC LAN8720A Module signals listed below will be terminated on the Module. The terminations follow the guidance given in the table below.

LAN8720A Signal Name	Series Termination	Parallel Termination	Notes
TXP (pin 21)		49.9ohm, 1.0% pull-up resistor to VDDA (created from +3.3V through a ferrite bead)	
TXN (pin 22)		49.9ohm, 1.0% pull-up resistor to VDDA	
RXP (pin 23)		49.9ohm, 1.0% pull-up resistor to VDDA	
RXN (pin 22)		49.9ohm, 1.0% pull-up resistor to VDDA	
LED1/REGOFF (pin 3)		10kohm, 1.0% pull-down resistor to ground.	
LED2/nINTSEL (pin 2)		10kohm,1.0% pull-down resistor to ground	

2.1.10. SDIO Interface

Sitara AM335x CPU is configured to support two MMC controllers. One is used for internal eMMC support, and the other is used for external SDHC/SDIO interface. The SMARC T335X module supports a 4bit SDIO interface, per the SMARC specification. The SDIO interface uses 3.3V signaling, per the SMARC spec and for compatibility with commonly available SDIO cards.
SDIO interface signals are exposed on the SMARC golden finger edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
G16	Mode0	MMC0_DAT0	P39	SDIO_D0	SDIO_D0	SDIO Data 0
G15	Mode0	MMC0_DAT1	P40	SDIO_D1	SDIO_D1	SDIO Data 1
F18	Mode0	MMC0_DAT2	P41	SDIO_D2	SDIO_D2	SDIO Data 2
F17	Mode0	MMC0_DAT3	P42	SDIO_D3	SDIO_D3	SDIO Data 3
V14	Mode7	GPIO1[17]	P33	SDIO_WP	MMC0_SDIO_WP	SDIO write protect signal
G18	Mode0	MMC0_CMD	P34	SDIO_CMD	SDIO_CMD	SDIO Command signal
U14	Mode7	GPIO1[18]	P35	SDIO_CD#	SDIO_CD#	SDIO card detect
G17	Mode0	MMC0_CLK	P36	SDIO_CK	SDIO_CK	SDIO Clock Signal
T14	Mode7	GPIO1[19]	P37	SDIO_PWR_EN	SDIO_PWREN	SD card power enable

The SDIO card power should be switched on the Carrier board and the SDIO lines should be ESD protected. The SMARC Evaluation Carrier schematic is useful as an implementation reference.

2.1.11. SPI Interface

The SMARC T335X module supports two AM335x SPI interfaces that are available off-Module for general purpose use. Each SPI channel has two chip-selects that can connect two SPI slave devices on each channel. Every device will share the "*SPI_DIN*", "*SPI_DO*" and "*SPI_CK*" pins, but each device will have its own chip select pin. The chip select signal is a low active signal.
The 4MB onboard SPI NOR flash uses the *SPI0_CS0#* signal. If a slave device would like to connect to SPI0 bus, use *SPI0_CS1#* instead. The onboard SPI NOR flash could be used as boot media or for users to store secure data in case that the file system on eMMC is crashed and the secure data could be restored. The schematic of SPI NOR flash is diagramed below.

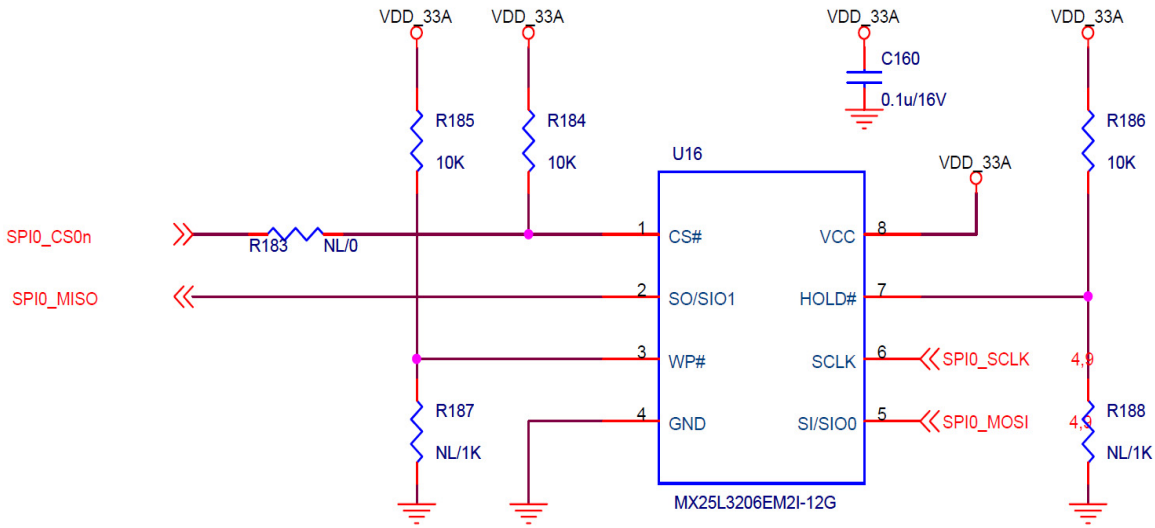


Figure 7: SPI Serial Flash Schematics

Note:
Use *SPI0_CS1#* chip select signal or SPI1 channel instead if users would like to have SPI slave devices on T335x carrier.

SPI interface signals are exposed on the SMARC golden finger edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
SPI0 Port						
A16	Mode0	SPI0_CS0	P43	SPI0_CS0#		SPI0 Master Chip Select 0 output, reserve for onboard NOR flash
C15	Mode0	SPI0_CS1	P31	SPI0_CS1#	SPI0_CS1#	SPI0 Master Chip Select 1 output
A17	Mode0	SPIO_SCLK	P44	SPI0_CK	SPI0_SCLK	SPI0 Master Clock output
B16	Mode0	SPI0_D1	P45	SPI0_DIN	SPI0_MISO	SPI0 Master Data input (input to CPU, output from SPI device)
B17	Mode0	SPI0_D0	P46	SDIO_DO	SPI0_MOSI	SPI0 Master Data output (output from CPU, input to SPI device)
SPI1 Port						
C12	Mode3	SPI1_CS0	P54	SPI1_CS0#	SPI1_CS0#	SPI1 Master Chip Select 0 output
A15	Mode4	SPI1_CS1	P55	SPI1_CS1#	SPI1_CS1#	SPI1 Master Chip Select 1 output
A13	Mode3	SPI1_SCLK	P56	SPI1_CK	SPI1_SCLK	SPI1 Master Clock output
D12	Mode3	SPI1_D1	P57	SPI1_DIN	SPI1_MISO	SPI1 Master Data input (input to CPU, output from SPI device)
B13	Mode3	SPI1_D0	P58	SDIO_DO	SPI1_MOSI	SPI1 Master Data output (output from CPU, input to SPI device)

2.1.12. I2S Interface

The SMARC T335X module supports one I2S interface. I2S is originated from Sitara AM335x McASP interface.

I2S interface signals are exposed on the SMARC T335X golden finger edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
D14	Mode0	XDMA_EVENT_INTR1	S38	Audio_MCK	AUD_MCLK	Master clock output to Audio codecs
C13	Mode3	MCASP1_FSX	S39	I2S0_LRCK	MCASP1_FSX	Left& Right audio synchronization clock
D13	Mode3	MCASP1_AXR0	S40	I2S0_SDOUT	MCASP1_AXR0	Digital audio Output
A14	Mode3	MCASP1_AXR1	S41	I2S0_SDIN	MCASP1_AXR1	Digital audio Input
B12	Mode3	MCASP1_ACLKX	S42	I2S0_CK	MCASP1_ACLKX	Digital audio clock

Note:
TLV320AIC3106 I2S audio codec is used in SmartBase T33 evaluation carrier board. An external 24.576 Mhz crystal is used as a reference clock output to audio codec instead of Pin S38. Theoretically, both ways will work.

2.1.13. Asynchronous Serial Port

The SMARC T335X module supports three UARTs (*SER0:1, 3*). UART *SER0* supports flow control signals (RTS, CTS). UART *SER1* and *SER3* do not support flow control. When working with software, *SER 3* is used for AM335x CPU debugging console port.
The module asynchronous serial port signals have a 3.3V level signal swing. They can be converted to RS232 level and polarity signals by using a suitable RS232 transceiver. Almost all transceivers available accept a 3.3V signal level: example include the Texas Instruments MAX3243. Note that RS232 transceivers invert the signal; a logic '1' is a negative voltage (-3.0V to -15V) and a logic '0' a positive voltage (3.0V to 15V) on the RS232 line. Asynchronous serial ports interface signals are exposed on the SMARC golden finger edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
SER0 Port						
E16	Mode0	UART0_TXD	P129	SER0_TX	SER0_TX	Asynchronous serial port data out
E15	Mode0	UART0_RXD	P130	SER0_RX	SER0_RX	Asynchronous serial port data in
E17	Mode0	UART0_RTSN	P131	SER0_RTS#	SER0_RTS#	Request to Send handshake line for SER0
E18	Mode0	UART0_CTSN	P132	SER0_CTS#	SER0_CTS#	Clear to Send handshake line for SER0
SER1 Port						
L18	Mode1	UART2_TXD	P134	SER1_TX	SER1_TX	Asynchronous serial port data out
K18	Mode1	UART2_RXD	P135	SER1_RX	SER1_RX	Asynchronous serial port data in
SER3 Port (Debugging Port)						
L16	Mode1	UART3_TXD	P140	SER3_TX	SER3_TX	Asynchronous serial port data out
L17	Mode1	UART3_RXD	P141	SER3_RX	SER3_RX	Asynchronous serial port data in

2.1.14. I2C Interface

There is a minimum configuration of I2C ports up to a maximum of 5 ports defined in the SMARC specification: PM (Power Management), LCD (Liquid Crystal Display), GP (General Purpose), CAM (Camera) and HDMI. SMARC T335x does not have camera and HDMI interface. It is therefore; the module defines only three I2C buses (PM, LCD and GP) and supports multiple masters and slaves in fast mode (400 KHz operation). This will be summarized below.

I2C Port		Primary Purpose	Alternative Use	I/O Voltage Level
Golden Finger Connector	AM335x CPU			
I2C_PM	I2C0	Power Management support	System configuration management	1.8V
I2C_GP	I2C1	General purpose use		3.3V
I2C_LCD	I2C2	LCD display support (for parallel and LVDS LCD)	General Purpose	3.3V

Note:

The 2.2k pull-up resistors for *I2C_SCL* and *I2C_SDA* signals are on module.

The I2C interface signals are exposed on the SMARC golden finger edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
PM_I2C						
C16	Mode0	I2C0_SCL	P121	I2C_PM_CK	I2C_PM_CK	Power management I2C bus clock
C17	Mode0	I2C0_SDA	P122	I2C_PM_DAT	I2C_PM_SDA	Power management I2C bus data
GP_I2C						
D15	Mode3	I2C1_SCL	S48	I2C_GP_CK	I2C_GP_CK	General purpose I2C bus clock
D16	Mode3	I2C1_SDA	S49	I2C_GP_DAT	I2C_GP_DAT	General purpose I2C bus data
LCD_I2C						
D17	Mode3	I2C2_SCL	S139	I2C_LCD_CK	I2C_LCD_CK	LCD display I2C bus clock
D18	Mode3	I2C2_SDA	S140	I2C_LCD_DAT	I2C_LCD_DAT	LCD display I2C bus data

All three I2C busses originate in the multi-master capable I2C controllers within the Sitara AM335x SoC. There are three I2C devices on the SMARC T335X Module are all on the *I2C_PM* (*I2C0*) bus and are operated at 1.8V. Those devices and their address details are listed in the following table:

#	Device	Description	Address (7-bit)	Address (8-bit)		Notes
				Read	Write	
I2C_PM Bus						
1	TI TPS65217C	PMIC	0x24	0x49	0x48	General purpose usage address
2	On Semiconductor CAT64C32	EEPROM	0x50	0xA1	0xA0	General purpose parameter EEPROM, Serial number, etc in PICMG EEEP format
3	Seiko S-35390A	Real-time clock IC	0x30	0x61	0x60	General purpose parameter with INT1 register access

As the name implies (*PM* == "*Power Management*"), this I2C bus is used by low level software for system power management. The Module PMIC TPS65217C power regulator is attached to this bus and various voltage levels and options are continuously modified over this interface. So - use care if accessing this interface.

Note:

The voltage level of *I2C_PM* on SMARC T335x is 1.8V. In Embedian Carrier design, the voltage level of *I2C_PM* will pull up to 3.3V (*I2C_PM_3V3*) on Carrier. Two more I2C devices are on *I2C_PM_3V3* bus in SmartBase T33 evaluation carrier board. Please refer to "***SMARC_T335x Carrier Board Hardware Design Guide***" and "***SMARC T335x Carrier Board User's Manual***" for details.

2.1.15. CAN Bus Interface

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control with a high level of security. The SMARC T335X module supports a CAN bus interface.
CAN interface signals are exposed on the SMARC golden finger edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
CAN BUS						
J18	Mode1	DCAN0_TX	P143	CAN0_TX	CAN0_TX	CAN0 Transmit output
K15	Mode1	DCAN0_RX	P144	CAN0_RX	CAN0_RX	CAN0 Receive input

By SMARC hardware specification, *CAN0* bus error condition signaling should be supported on the Module *GPIO8* (*P116*) pin. This is an active low input to the Module from the CAN bus transceiver.
A CAN transceiver on carrier is necessary to adapt the signals from SMARC golden finger edge connector, which is TTL levels, to the physical layer used. Because the CAN bus system is typically used to connect multiple systems and is often run over very long distances, both power supply and signal path must be electrically isolated to meet a certain isolation level. Users can refer the "***SMARC_T335x Carrier Board Hardware Design Guide***" or CAN transceiver application note such as TI ISO1050 for more details.

2.1.16. GPIOs

The SMARC T335X module supports 12 GPIOs, per the SMARC specification. Specific alternate functions are assigned to some GPIOs such as PWM / Tachometer capability, Camera support, CAN Error Signaling and HD Audio reset. All pins are capable of bi-directional operation. A default direction of operation is assigned, with half of them (GPIO0 – GPIO5) for use as outputs and the remainder (GPIO6 – GPIO11) as inputs by SMARC hardware specification. GPIO signals are exposed on the SMARC golden finger edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
GPIOs						
J17	Mode7	GPIO3[4]	P108	GPIO0/CAM0_PWR#	GPIO0	Camera 0 Power Enable, active low output
C18	Mode7	GPIO0[7]	P109	GPIO1/CAM1_PWR#	GPIO1	Camera 1 Power Enable, active low output
U16	Mode7	GPIO1[25]	P110	GPIO2/CAM0_RST#	GPIO2	Camera 0 Reset, active low output
V16	Mode7	GPIO1[24]	P111	GPIO3/CAM1_RST#	GPIO3	Camera 1 Reset, active low output
U6	Mode7	GPIO2[4]	P112	GPIO4/HDA_RST#	GPIO4	HD Audio Reset, active low output
T7	Mode7	GPIO2[3]	P113	GPIO5/PWM_OUT	GPIO5	PWM output
U18	Mode7	GPIO1[28]	P114	GPIO6/TACHIN	GPIO6	Tachometer input (used with the GPIO5 PWM)
V6	Mode7	GPIO1[29]	P115	GPIO7/PCAM_FLD	GPIO7	PCAM_FLD (Field) signal input
T13	Mode7	GPIO2[0]	P116	GPIO8/CAN0_ERR#	GPIO8	CAN0 Error signal, active low input
V12	Mode7	GPIO2[1]	P117	GPIO9/CAN1_ERR#	GPIO9	CAN1 Error signal, active low input
C14	Mode7	GPIO3[7]	P118	GPIO10	GPIO10	
B14	Mode7	GPIO3[8]	P119	GPIO11	GPIO11	

2.1.17. 4-wire Resistive Touch Interface

Resistive touch interface is not defined in SMARC hardware specification. However, to support legacy touch devices, SMARC T335x has 4-wire resistive touch interface on AFB (Alternative Function Block) pins.

Touchscreen controller on Sitara AM335x is an 8 channel general purpose ADC, with support for interleaving Touch Screen conversions for a 4-wire resistive panel. A resistive touchscreen operates by applying a voltage across a resistive network and measuring the change in resistance at a given point on the matrix where the screen is touched by an input (stylus or finger). The change in the resistance ratio marks the location on the touchscreen.
4-wire TSC has been implemented on SMARC T335X module. TSC signals are exposed on the SMARC golden finger edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
4-wire TSC						
B6		AIN0	S18	AFB1_OUT	XPUL	XP: Plus X-axis on-off control signal
B7		AIN2	S19	AFB2_OUT	YPLL	YP: Plus Y-axis on-off control signal
C7		AIN1	S21	AFB4_IN	XNUR	XM: Minus X-axis on-off control signal
A7		AIN3	S22	AFB5_IN	YNLR	YM: Minus Y-axis on-off control signal

2.1.18. Watchdog Timer Interface

Sitara AM335x features an internal WDT. Embedian's Linux kernel enables the internal AM335x WDT and makes this functionality available to users through the standard Linux Watchdog API.
A description of the API is available following the link below:
http://www.kernel.org/doc/Documentation/watchdog/watchdog-api.txt

WDT signals are exposed on the SMARC golden finger edge connector as shown below:

TI AM335x CPU			SMARC T335X Edge Golden Finger		Net Names	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
Watchdog Timer						
R7	Mode2	Timer4	S145	WDT_TIME_OUT#	WDT_TIMER_OUT#	Watchdog-Timer Output

2.1.19. JTAG

Figure 8 shows the SMARC T335x JTAG connectors location and pin out.

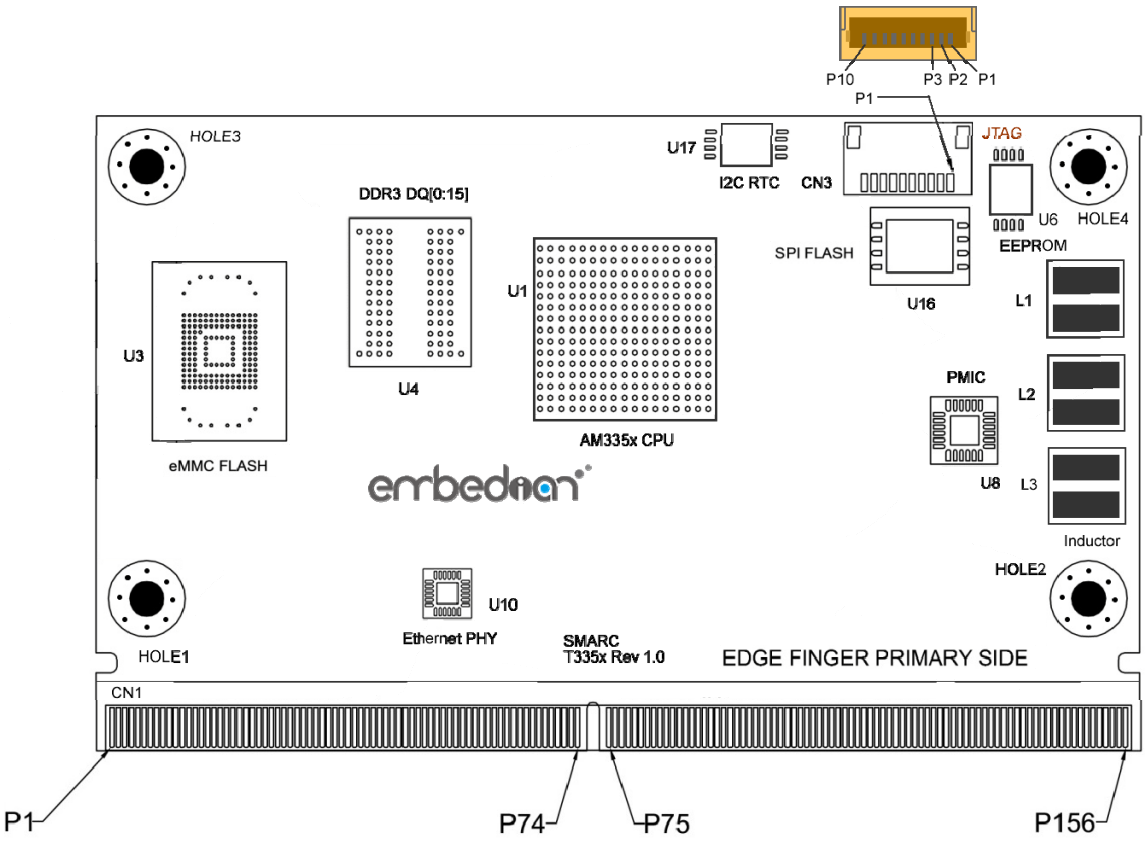


Figure 8: JTAG Connector Location and Pinout

JTAG functions for CPU debug and test are implemented on separate small form factor connector (CN3: *JST SM10B-SRSS-TB*, 1mm pitch R/A SMD Header). The JTAG pins are used to allow test equipment and circuit emulators to have access to the Module CPU. The pin-outs shown below are used:

TI AM335x CPU			CN3 (Connector: JST SM10B-SRSS-TB, 1mm pitch R/A SMD Header)		Type	Note
Ball	Mode	Pin Name	Pin#	Pin Name		
JTAG						
			1	VDD_33A	Power	JTAG I/O Voltage (sourced by Module)
B10		nTRST	2	nTRST	I	JTAG Reset, active low
C11		TMS	3	TMS	I	JTAG mode select
A11		TDO	4	TDO	O	JTAG data out
B11		TDI	5	TDI	I	JTAG data in
A12		TCK	6	TCK	I	JTAG clock
			7	RTCK	I	JTAG return clock
			8	GND	Ground	Ground
			9	MFG_Mode#	I	Pulled low to allow in-circuit SPI ROM update
			10	GND	Ground	Ground

2.1.20. Boot ID EEPROM

The SMARC T335x module includes an I2C serial EEPROM available on the I2C_PM bus. An On Semiconductor 24C32 or equivalent EEPROM is used in the module. The device operates at 1.8V. The Module serial EEPROM is placed at I2C slave addresses A2 A1 A0 set to 0 (I2C slave address 50 hex, 7 bit address format or A0 / A1 hex, 8 bit format) (for I2C EEPROMs, address bits A6 A5 A4 A3 are set to binary 0101 convention).

The module serial EEPROM is intended to retain module parameter information, including serial number. The module serial EEPROM data structure conforms to the PICMG® EEEP Embedded EEPROM Specification.

Note:
The EEPROM ID memory layout is now follow the mainline and as follows.

Name	Size (Bytes)	Contents
Header	4	MSB 0xEE3355AA LSB
Board Name	8	Name for Board in ASCII "SMARCT33" = Embedian SMARC T335X Computer on Module
Version	4	Hardware version code for version in ASCII "00A0" = rev. A0
Serial Number	12	Serial number of the board. This is a 12 character string which is: MSCEWWYYnnnn Where: WW = 2 digit week of the year of production YY = 2 digit year of production nnnn = incrementing board number
Configuration Option	32	Codes to show the configuration setup on this board. For the available T335X supported, the following codes are used: ASCII = "SMARCT33" = default configuration Remaining 24 bytes are reserved
Available	32720	Available space for other non-volatile codes/data

After 00A0 version, the EEPROM will be write-protected.

2.2 SMARC T335X Debug

2.2.1. Serial Port Debug

SMARC module has 3 serial output ports, SER0, SER1, and SER3. Out of these 3 serial ports, SER3 is set as the serial debug port use for Sitara AM335x. SER3 is exposed (along with all other serial ports available on the module) in the SMARC T335X Evaluation Carrier. The default baud rate setting is 115,200 8N1.
SER3 pin out of the SMARC T335X is shown below:

TI AM335x CPU		SMARC T335X Edge Golden Finger		Net Names	Notes
mode	Pin Name	Pin#	Pin Name		
SER1 (Debugging Port)					
Mode1	UART3_TXD	P140	SER3_TX	SER3_TX	Asynchronous serial port data out
Mode1	UART3_RXD	P141	SER3_RX	SER3_RX	Asynchronous serial port data in

2.3 Mechanical Specifications

2.3.1. Module Dimensions

The SMARC T335X complies with SMARC Hardware Specification in an 82mm x 50 mm form factor.

2.3.2. Height on Top

2.9mm maximum (without PCB) complied with SMARC specification defines as 3mm as the maximum.

2.3.3. Height on Bottom

0.9mm maximum (without PCB) complied with SMARC specification defines as 1.3mm as the maximum.

2.3.4. Mechanical Drawings

The mechanical information is shown in Figure 9: SMARC T335X Mechanical Drawings (Top View) and Figure 10: SMARC T335X Mechanical Drawings (Bottom View))

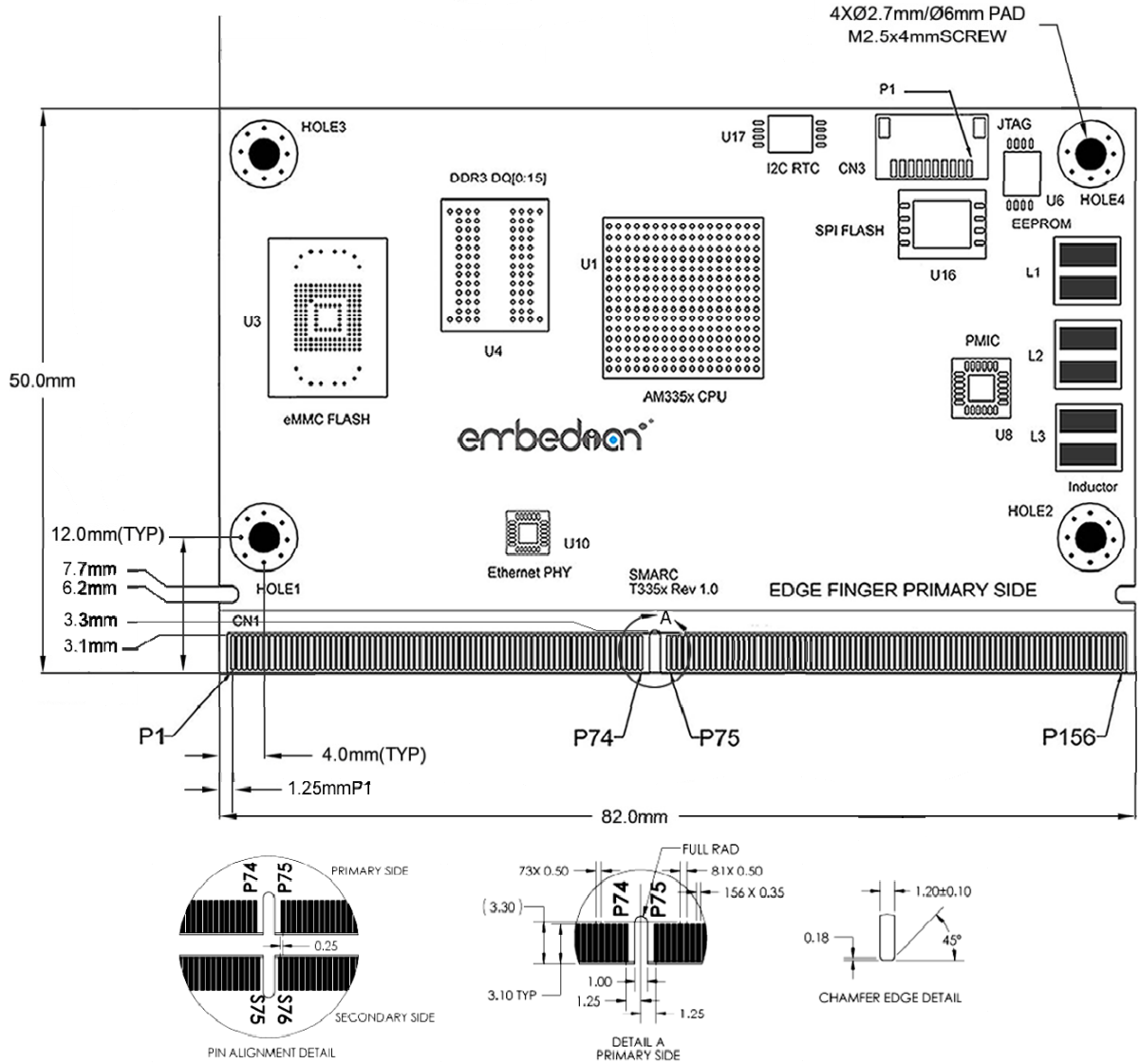


Figure 9. SMARC T335X Mechanical Drawings (Top View)

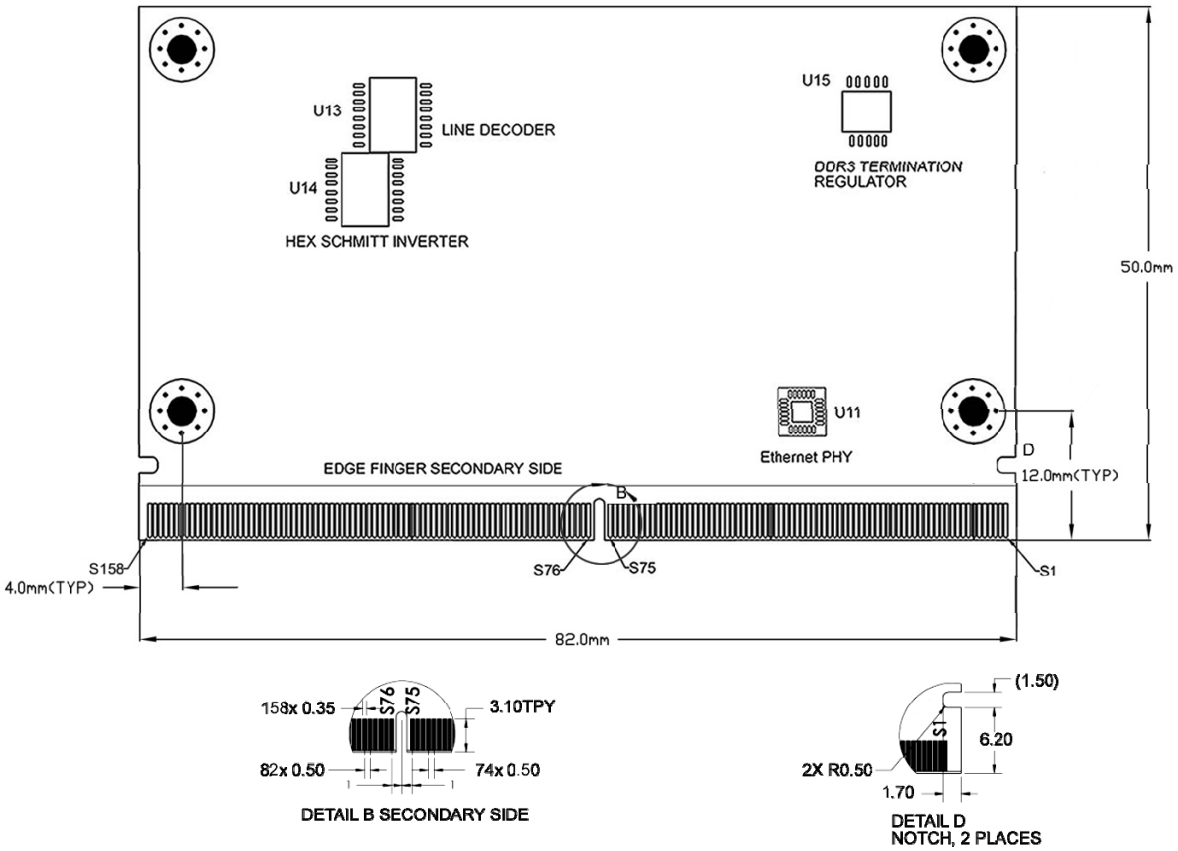


Figure 10. SMARC T335X Mechanical Drawings (Bottom View)

Top side major component (IC and Connector) information is shown in Figure 11: SMARC T335X Top side components.

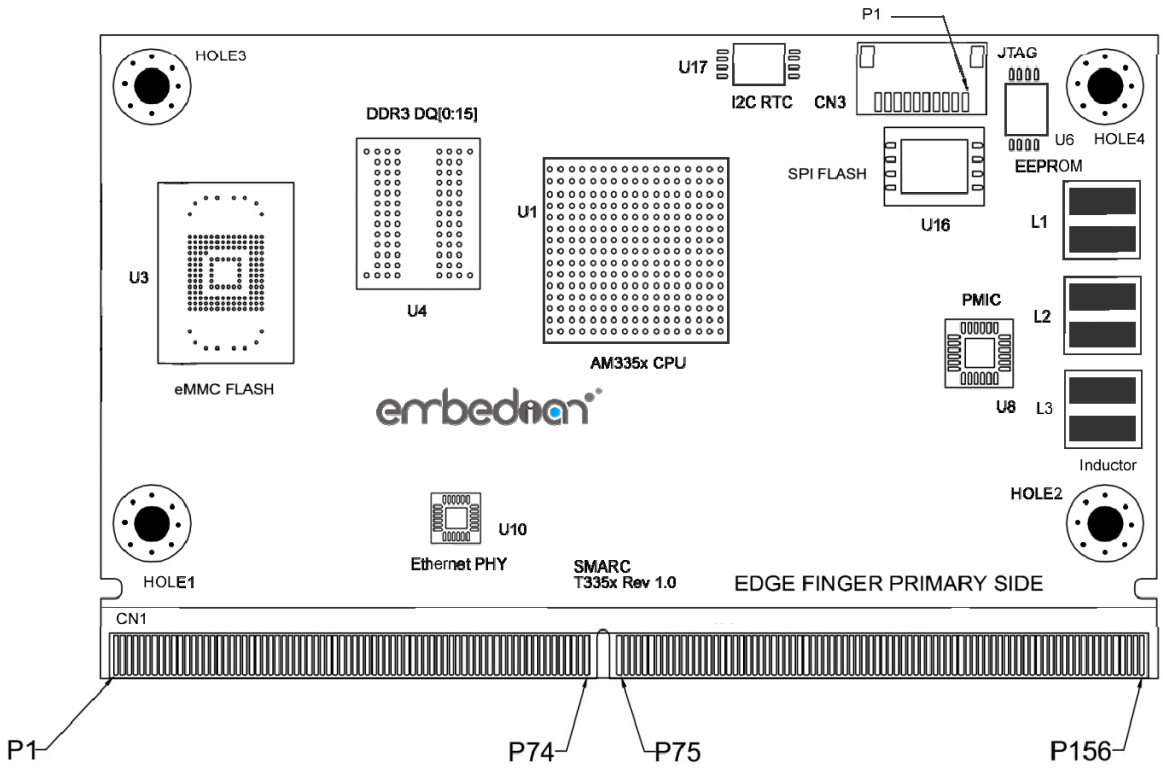


Figure 11. SMARC T335X Top Side Components

Bottom side major component (IC and Connector) information is shown in Figure 12: SMARC T335X Bottom side components.

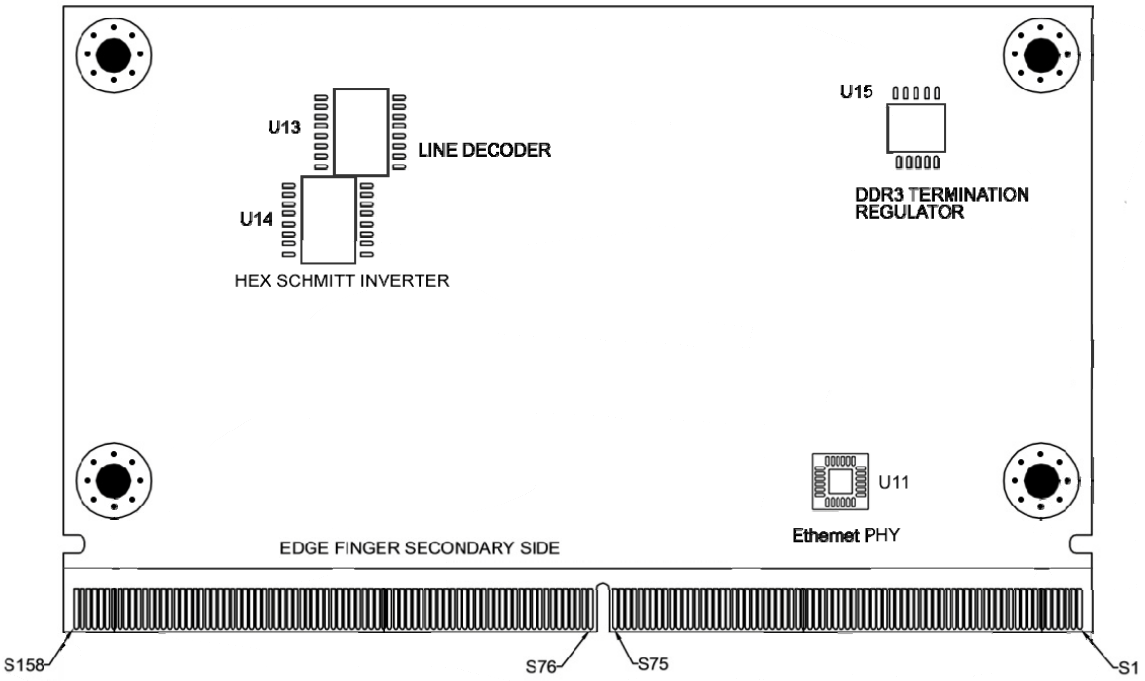


Figure 12. SMARC T335X Bottom Side Components

SMARC T335x height information from Carrier board Top side to tallest Module component is shown in Figure 13: SMARC T335x Minimum "Z" Height:

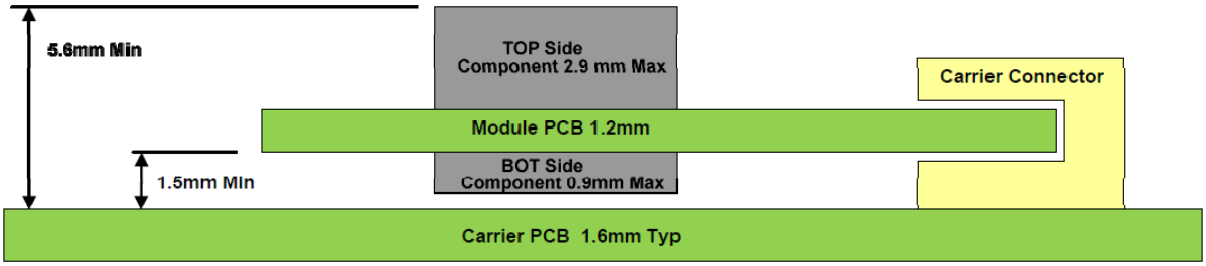


Figure 13. SMARC T335x Minimum "Z" Height

The SMARC connector board-to-board stack heights that are available may result in the use of non-standard spacer lengths. The board-to-board stack heights available include 1.5mm, 2.7mm and 5mm. Of these three, only the spacer for the 5mm stack would likely be a standard length.
When a 1.5mm stack height Carrier board connector is used, there shall not be components on the Carrier board Top side in the Module region. Additionally, when 1.5mm stack height connectors are used, there should not be PCB traces on the Carrier top side in the Module shadow. This is to prevent possible problems with metallic Module heat sink attachment

hardware that may protrude through the Module.
If Carrier board components are required in this region, then the Carrier components must be on the Carrier Bottom side, or a taller Module-to-Carrier connector may be used. Stack heights of 2.7mm, 3mm, 5mm and up are available.

2.3.5. MTBF

The SMARC T335X System MTBF (hours) : >100,000 hours

The above MTBF (Mean Time Between Failure) values were calculated using a combination of manufacturer's test data, if the data was available, and a Bellcore calculation for the remaining parts. The Bellcore calculation used is "Method 1 Case 1". In that particular method the components are assumed to be operating at a 50 % stress level in a 40° C ambient environment and the system is assumed to have not been burned in. Manufacturer's data has been used wherever possible. The manufacturer's data, when used, is specified at 50°C, so in that sense the following results are slightly conservative. The MTBF values shown below are for a 40°C in an office or telecommunications environment. Higher temperatures and other environmental stresses (extreme altitude, vibration, salt water exposure, etc.) lower MTBF values.

2.3.6. Module Assembly Hardware

The SMARC T335X module is attached to the carrier with four M2.5 screws. A 4mm length screw is usually used. The attachment holes are located on the corners of the module. Attachment holes have a 6mm diameter pad, 2.7 mm dia drill hole as shown Figure 8: SMARC T335X Mechanical Drawings (Top View)

2.3.7. Module Cooling Solution

Sitara AM335x is a low heat dissipation processor. The module implementations on TI devices benefit from the low-power architecture of TI's Sitara™ ARM® MPU platform, which eliminates the need for a fan or heat sink. In most use cases, the peak power of AM335x ARM MPUs is under 1W.

2.4 Electrical Specifications

2.4.1. Supply Voltage

The SMARC T335X module operates over an input voltage range of 3.35V to 5.25V. Power is provided from the carrier through 10 power pins as defined by the SMARC specification.

Caution! The SMARC specification states that the input voltage range should extend down to 3.0V. The SMARC T335X lower limit is determined by a non-volatile register setting in the TI PMIC used and is set 3.35V by default. A single 5V DC input is recommended.

2.4.2. RTC/Backup Voltage

3.0V RTC backup power is provided through the VDD_RTC pin from the carrier board. This connection provides back up power to the module PMIC. The RTC is powered via the primary system 3.3V supply during normal operation and via the VBAT power input, if it is present, during power-off.

2.4.3. No Separate Standby Voltage

The SMARC T335X does not have a standby power rail. Standby operation is powered through the main supply voltage rail, as defined in the SMARC specification.

2.4.4. Module I/O Voltage

The SMARC T335X module supports 3.3V level I/O voltage only as defined by SMARC Hardware specification. Module pin S158 (*VDD_IO_SEL#*) is tied high through a resistance of 100K on the Module, per the SMARC specification, indicating a 3.3V I/O voltage level. The SmartBase T33 evaluation carrier also supports 3.3V I/O SMARC module only.

2.4.5. Power Consumption

Power consumption is highly dependent on the individual user's application; however, this section focuses on typical SMARC T335X application-usage case scenarios and the environment settings that were used to perform such power measurements. Power figures are given in the table below for the Module power consumption. These are Module power figures. Off-Module power consumption (e.g. display backlight, display power, Carrier board devices) is not included here. What is included in these power figures: everything on the Module – the TI Sitara SoC, the DDR3 DRAM, the eMMC memory, the Module power supplies, the fast LAN PHY and miscellaneous Module circuits. The figures below given below are subject to change.

Software : Linux (No application running after boot)
Use Case : Command prompt after login, No application running
OPP : OPP100 (ARM 550 MHz, DDR 200 MHz, L3 200 MHz, L4 100 MHz)
Measured DMIPS/MHz : 1.8 ~ 1.9 DMIPS/MHz

Power Supply	Nominal Rating	Voltage Drop [mV]	Voltage [V]	Current [mA]	Power [mW]
VDD_CORE	1.1V +/-4%	9.10	1.094	181.92	198.97
VDD_MPU	1.1V – 1.3V +/-4%	5.56	1.104	111.20	122.73
VDDS_RTC	1.8V +/-5%	0.72	1.800	0.36	0.65
VDDS_DDR	1.8V +/-5% / 1.5V +/-5%	9.03	1.793	37.62	67.44
VDDS	1.8V +/-5%	0.13	1.796	0.55	1.00
VDDS_SRAM_CORE_BG	1.8V +/-5%	2.66	1.809	1.33	2.40
VDDS_SRAM_MPU_BB	1.8V +/-5%	2.70	1.809	1.35	2.44
VDDS_PLL_DDR	1.8V +/-5%	1.69	1.810	0.84	1.52
VDDS_PLL_CORE_LCD	1.8V +/-5%	15.98	1.797	7.99	14.36
VDDS_PLL_MPU	1.8V +/-5%	3.38	1.809	1.69	3.05
VDDS_OSC	1.8V +/-5%	1.33	1.811	0.67	1.21
VDDA1P8V_USB0/1	1.8V +/-5%	16.15	1.801	16.15	29.07
VDDA3P3V_USB0/1	3.3V +/-5%	5.21	3.309	2.61	8.62
VDDA_ADC	1.8V +/-5%	0.45	1.816	0.45	0.82
VDDSHV1	1.8 / 3.3 V +/-5%	0.02	3.324	0.08	0.28
VDDSHV2	1.8 / 3.3 V +/-5%	0.00	3.292	0.00	0.00
VDDSHV3	1.8 / 3.3 V +/-5%	0.01	3.325	0.06	0.19
VDDSHV4	1.8 / 3.3 V +/-5%	0.01	3.292	0.03	0.11
VDDSHV5	1.8 / 3.3 V +/-5%	0.93	3.323	3.89	12.92
VDDSHV6	1.8 / 3.3 V +/-5%	1.35	3.322	5.64	18.73
				Total	**486.51**

2.5 Environmental Specifications

2.5.1. Operating Temperature

The SMARC T335x module operates from 0°C to 60°C air temperature, without a passive heat sink arrangement. Industrial temperature (-40°C ~85°C is also available with different part number SMARC T335x-I).

2.5.2. Humidity

Operating: 10% to 90% RH (non-condensing).
Non-operating: 5% to 95% RH (non-condensing).

2.5.3. ROHS Compliance

The SMARC T335x module is compliant to the 2002/95/EC RoHS directive.

Connector PinOut

This Chapter gives detail pinout of SMARC T335X golden finger edge connector.

Section include：

- SMARC T335X Connector Pin Mapping

Chapter 3 Connector Pinout

The Module pins are designated as P1 – P156 on the Module Primary (Top) side, and S1 – S158 on the Module Secondary (Bottom) side. There are total of 314 pins on the Module. The connector is sometimes identified as a 321 pin connector, but 7 pins are lost to the key (4 on the primary side and 3 on secondary side).

The Secondary (Bottom) side faces the Carrier board when a normal or standard Carrier connector is used.

The SMARC T335x module pins are deliberately numbered as P1 – P156 and S1 – S158 for clarity and to differentiate the SMARC Module from MXM3 graphics modules, which use the same connector but use the pins for very different functions. MXM3 cards and MXM3 baseboard connectors use different pin numbering scheme.

3.1 SMARC T335X Connector Pin Mapping

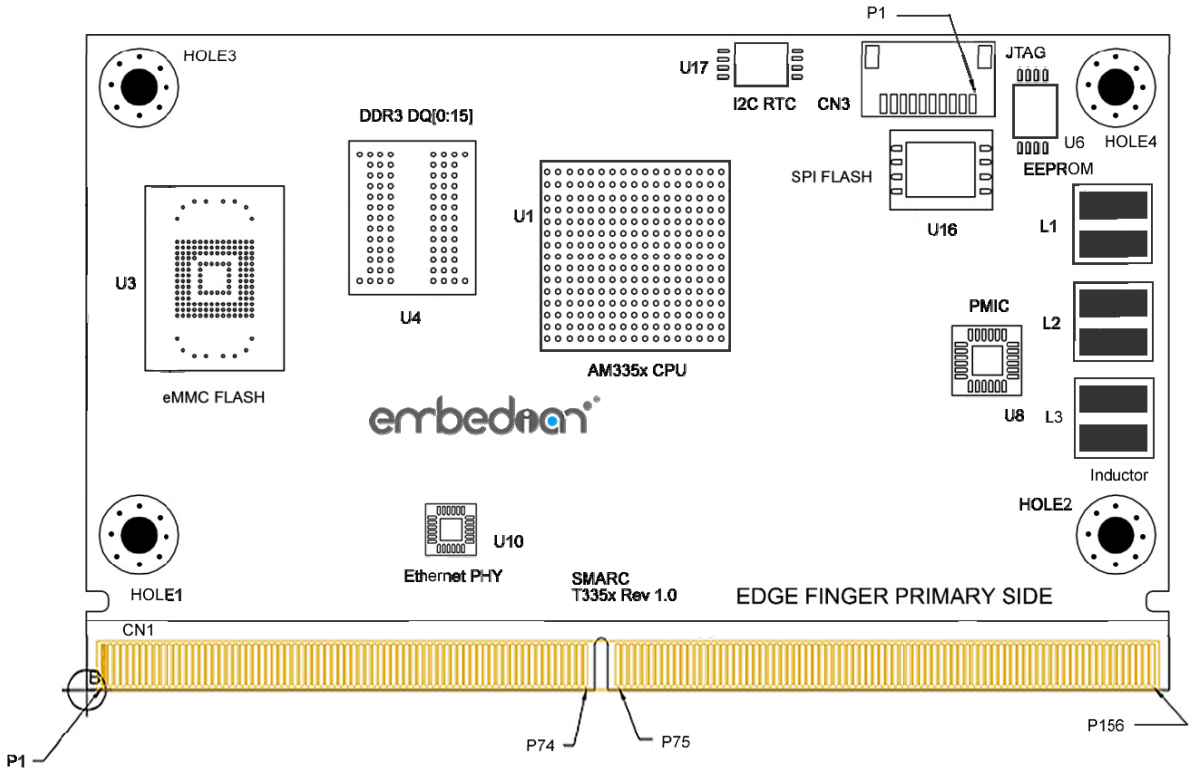


Figure 14: SMARC T335X edge finger primary pins

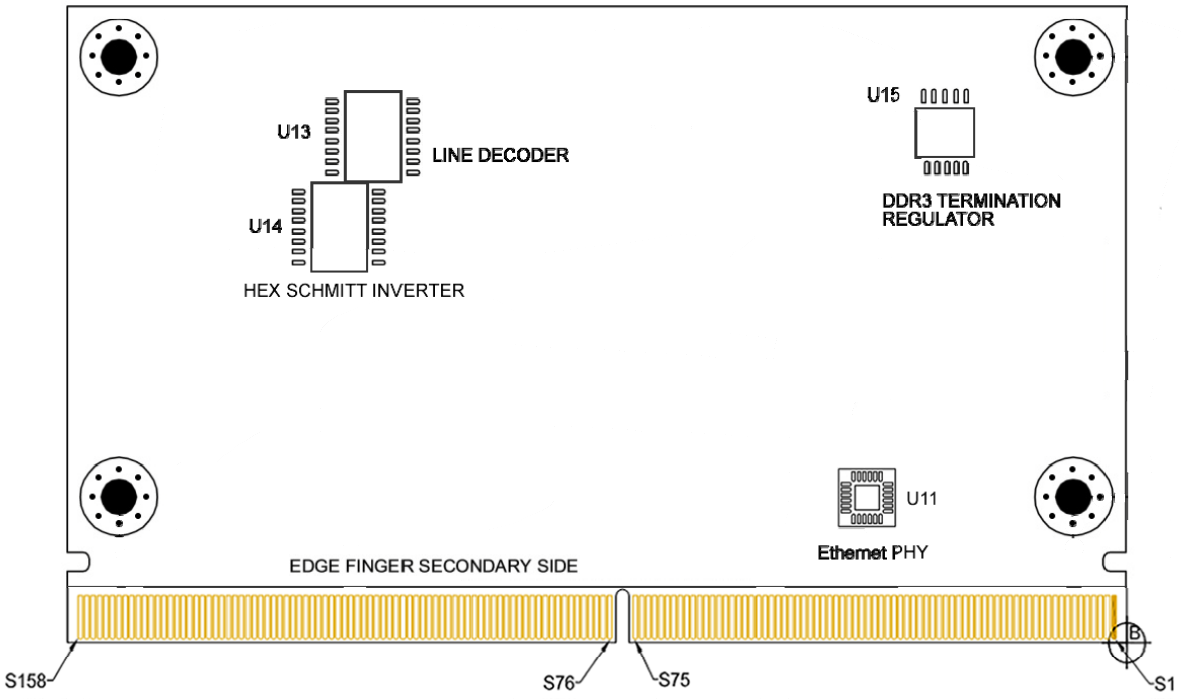


Figure 15: SMARC T335X edge finger secondary pins

The next tables describe each pin, its properties, and its use on the module and development board.
The "*SMARC Edge Finger*" column shows the connection of the signals defined in the SMARC specification. The "*Sitara AM335x CPU*" column shows the connection of the CPU signals on the module. The format of this column is "*Ball/Mode/Signal Name*" where "*Signal Name*" is the chip where the signals are connected, and "*Ball*" is the name of the pad where the signals are connected as they are defined in the AM335x's datasheet.

Pinout Legend

I	*Input*
O	*Output*
I/O	*Input or output*
P	*Power*
AI	*Analogue input*
AO	*Analogue output*
AIO	*Analogue Input or analogue output*
OD	*Open Drain Signal*
#	*Low level active signal*

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P1	PCAM_PXL_CK1					Not used
P2	GND				P	Ground
P3	CSI1_CK+ / PCAM_D0					Not used
P4	CSI1_CK- / PCAM_D1					Not used
P5	PCAM_DE					Not used
P6	PCAM_MCK					Not used
P7	CSI1_D0+ / PCAM_D2					Not used
P8	CSI1_D0- / PCAM_D3					Not used
P9	GND				P	Ground
P10	CSI1_D1+ / PCAM_D4					Not used
P11	CSI1_D1- / PCAM_D5					Not used
P12	GND				P	Ground
P13	CSI1_D2+ / PCAM_D6					Not used
P14	CSI1_D2- / PCAM_D7					Not used
P15	GND				P	Ground
P16	CSI1_D3+ / PCAM_D8					Not used
P17	CSI1_D3- / PCAM_D9					Not used
P18	GND				P	Ground
P19	GbE_MDI3-					Not used

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P20	GbE_MDI3+					Not used
P21	GbE_LINK100#				O OD	SMSC LAN8720A and OD driver
P22	GbE_LINK1000#					Not used
P23	GbE_MDI2-					Not used
P24	GbE_MDI2+					Not used
P25	GbE_LINK_ACT#				O OD	SMSC LAN8720A and OD driver
P26	GbE_MDI1-				AIO	SMSC LAN8720A: Differential Transmit/Receive Negative Channel 1
P27	GbE_MDI1+				AIO	SMSC LAN8720A: Differential Transmit/Receive Positive Channel 1
P28	GbE1_CTREF				O	SMSC LAN8720A Center tap reference voltage for GBE Carrier board Ethernet magnetic
P29	GbE_MDI0-				AIO	SMSC LAN8720A: Differential Transmit/Receive Negative Channel 0
P30	GbE_MDI0+				AIO	SMSC LAN8720A: Differential Transmit/Receive Positive Channel 0

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P31	SPI0_CS1#	C15	Mode0	SPI0_CS1	O	SPI0 Master Chip Select 1 output.
P32	GND				P	Ground
P33	SDIO_WP	V14	Mode0	GPIO1[17]	I	Write Protect
P34	SDIO_CMD	G18	Mode0	MMC0_CMD	IO	Command Line
P35	SDIO_CD#	U14	Mode7	GPIO1[18]	I	Card Detect
P36	SDIO_CK	G17	Mode0	MMC0_CLK	O	Clock
P37	SDIO_PWR_EN	T14	Mode7	GPIO1[19]	O	SD card power enable
P38	GND				P	Ground
P39	SDIO_D0	G16	Mode0	MMC0_DAT0	IO	Data path
P40	SDIO_D1	G15	Mode0	MMC0_DAT1	IO	Data path
P41	SDIO_D2	F18	Mode0	MMC0_DAT2	IO	Data path
P42	SDIO_D3	F17	Mode0	MMC0_DAT3	IO	Data path
P43	SPI0_CS0#	A16	Mode0	SPI0_CS0	O	SPI0 Master Chip Select 0 output, reserved for on-module NOR flash
P44	SPI0_CK	A17	Mode0	SPIO_SCLK	O	SPI0 Master Clock output
P45	SPI0_DIN	B16	Mode0	SPI0_D1	I	SPI0 Master Data input (input to CPU, output from SPI device)
P46	SPI0_DO	B17	Mode0	SPI0_D0	O	SPI0 Master Data output (output from CPU, input to SPI device)

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P47	GND				P	Ground
P48	SATA_TX+					Not used
P49	SATA_TX-					Not used
P50	GND				P	Ground
P51	SATA_RX+					Not used
P52	SATA_RX-					Not used
P53	GND				P	Ground
P54	SPI1_CS0#	C12	Mode3	SPI1_CS0	O	SPI1 Master Chip Select 0 output
P55	SPI1_CS1#	A15	Mode4	SPI1_CS1	O	SPI1 Master Chip Select 1 output
P56	SPI1_CK	A13	Mode3	SPI1_SCLK	O	SPI1 Master Clock output
P57	SPI1_DIN	D12	Mode3	SPI1_D1	I	SPI1 Master Data input (input to CPU, output from SPI device)
P58	SPI1_DO	B13	Mode3	SPI1_D0	O	SPI1 Master Data output (output from CPU, input to SPI device)
P59	GND				P	Ground
P60	USB0+	N17	Mode0	USB0_DP	IO	Differential USB0 data
P61	USB0-	N18	Mode0	USB0_DM	IO	Differential USB0 data

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P62	USB0_EN_OC#	F16	Mode0	USB0DRVVBUS	IO OD	Pulled low by Module OD driver to disable USB0 power Pulled low by Carrier OD driver to indicate over-current situation If this signal is used, a pull-up is required on the Carrier
P63	USB0_VBUS_DET	P15	Mode0	USB0_VBUS	I	USB host power detection, when this port is used as a device
P64	USB0_OTG_ID	P16	Mode0	USB0_ID	I	USB OTG ID input, active high
P65	USB1+	R18	Mdde0	USB1_DP	IO	Differential USB0 data pair
P66	USB1-	R17	Mode0	USB1_DM	IO	
P67	USB1_EN_OC#	F15	Mode0	USB1DRVVBUS	IO OD	Pulled low by Module OD driver to disable USB0 power Pulled low by Carrier OD driver to indicate over-current situation If this signal is used, a pull-up is required on the Carrier

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P68	GND				P	Ground
P69	USB2+					Not used
P70	USB2-					Not used
P71	USB2_EN_OC#					Not used
P72	PCIE_C_PRSNT#					Not used
P73	PCIE_B_PRSNT#					Not used
P74	PCIE_A_PRSNT#					Not used
P75	PCIE_A_RST#					Not used
P76	PCIE_C_CKREQ#					Not used
P77	PCIE_B_CKREQ#					Not used
P78	PCIE_A_CKREQ#					Not used
P79	GND				P	Ground
P80	PCIE_C_REFCK+					Not used
P81	PCIE_C_REFCK-					Not used
P82	GND				P	Ground
P83	PCIE_A_REFCK+					Not used
P84	PCIE_A_REFCK-					Not used
P85	GND				P	
P86	PCIE_A_RX+					Not used
P87	PCIE_A_RX-					Not used
P88	GND				P	Ground
P89	PCIE_A_TX+					Not used
P90	PCIE_A_TX-					Not used

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P91	GND				P	Ground
P92	HDMI_D2+					Not used
P93	HDMI_D2-					Not used
P94	GND				P	Ground
P95	HDMI_D1+					Not used
P96	HDMI_D1-					Not used
P97	GND				P	Ground
P98	HDMI_D0+					Not used
P99	HDMI_D0-					Not used
P100	GND				P	Ground
P101	HDMI_CK+					Not used
P102	HDMI_CK-					Not used
P103	GND				P	Ground
P104	HDMI_HPD					Not used
P105	HDMI_CTRL_CK					Not used
P106	HDMI_CTRL_DAT					Not used
P107	HDMI_CEC					Not used
P108	GPIO0 / CAM0_PWR#	J17	Mode7	GPIO3[4]	IO	Camera 0 Power Enable, active low output
P109	GPIO1 / CAM1_PWR#	C18	Mode7	GPIO0[7]	IO	Camera 1 Power Enable, active low output
P110	GPIO2 / CAM0_RST#	U16	Mode7	GPIO1[25]	IO	Camera 0 Reset, active low output

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P111	GPIO3 / CAM1_RST#	V16	Mode7	GPIO1[24]	IO	Camera 1 Reset, active low output
P112	GPIO4 / HDA_RST#	U6	Mode7	GPIO2[4]	IO	HD Audio Reset, active low output
P113	GPIO5 / PWM_OUT	T7	Mode7	GPIO2[3]	IO	PWM output
P114	GPIO6 / TACHIN	U18	Mode7	GPIO1[28]	IO	Tachometer input (used with the GPIO5 PWM)
P115	GPIO7 / PCAM_FLD	V6	Mode7	GPIO1[29]	IO	PCAM_FLD (Field) signal input
P116	GPIO8 / CAN0_ERR#	T13	Mode7	GPIO2[0]	IO	CAN0 Error signal, active low input
P117	GPIO9 / CAN1_ERR#	V12	Mode7	GPIO2[1]	IO	CAN1 Error signal, active low input
P118	GPIO10	C14	Mode7	GPIO3[7]	IO	
P119	GPIO11	B14	Mode7	GPIO3[8]	IO	
P120	GND				P	
P121	I2C_PM_CK	C16	Mode0	I2C0_SCL	IO OD	Power management I2C bus clock
P122	I2C_PM_DAT	C17	Mode0	I2C0_SDA	IO OD	Power management I2C bus data
P123	BOOT_SEL0#				I	SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier.

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P124	BOOT_SEL1#				I	SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier.
P125	BOOT_SEL2#				I	SYSBOOT and Line De-multiplexer Logic Pulled up on Module. Driven by OD part on Carrier.
P126	RESET_OUT#				O	PMIC TPS65217C and Reset Logic, General purpose reset output to Carrier board.
P127	RESET_IN#				I	PMIC TPS65217C through Level Translator, Reset input from Carrier board. Carrier drives low to force a Module reset, floats the line otherwise Pulled up on Module. Driven by OD part on Carrier.

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P128	POWER_BTN#				I	PMIC TPS65217C, Power-button input from carrier board. Carrier to float the line in in-active state. Active low, level sensitive. It is de-bounced on the Module Pulled up on Module. Driven by OD part on Carrier.
P129	SER0_TX	E16	Mode0	UART0_TXD	O	Asynchronous serial port data out
P130	SER0_RX	E15	Mode0	UART0_RXD	I	Asynchronous serial port data in
P131	SER0_RTS#	E17	Mode0	UART0_RTSN	O	Request to Send handshake line for SER0
P132	SER0_CTS#	E18	Mode0	UART0_CTSN	I	Clear to Send handshake line for SER0
P133	GND				P	Ground
P134	SER1_TX	L18	Mode1	UART2_TXD	O	Asynchronous serial port data out
P135	SER1_RX	K18	Mode1	UART2_RXD	I	Asynchronous serial port data in
P136	SER2_TX					Not used
P137	SER2_RX					Not used
P138	SER2_RTS#					Not used
P139	SER2_CTS#					Not used

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
P140	SER3_TX	L16	Mode1	UART3_TXD	O	Asynchronous serial port data out
P141	SER3_RX	L17	Mode1	UART3_RXD	I	Asynchronous serial port data in
P142	GND				P	Ground
P143	CAN0_TX	J18	Mode1	DCAN0_TX	O	CAN0 Transmit output
P144	CAN0_RX	K15	Mode1	DCAN1_RX	I	CAN0 Receive input
P145	CAN1_TX					Not used
P146	CAN1_RX					Not used
P147	VDD_IN				P	Power in
P148	VDD_IN				P	Power in
P149	VDD_IN				P	Power in
P150	VDD_IN				P	Power in
P151	VDD_IN				P	Power in
P152	VDD_IN				P	Power in
P153	VDD_IN				P	Power in
P154	VDD_IN				P	Power in
P155	VDD_IN				P	Power in
P156	VDD_IN				P	Power in

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S1	PCAM_VSYNC					Not used
S2	PCAM_HSYNC					Not used
S3	GND				P	Ground
S4	PCAM_PXL_CK0					Not used
S5	I2C_CAM_CK					Not used
S6	CAM_MCK					Not used
S7	I2C_CAM_DAT					Not used
S8	CSI0_CK+ / PCAM_D10					Not used
S9	CSI0_CK- / PCAM_D11					Not used
S10	GND				P	Ground
S11	CSI0_D0+ / PCAM_D12					Not used
S12	CSI0_D0- / PCAM_D13					Not used
S13	GND				P	Ground
S14	CSI0_D1+ / PCAM_D14					Not used
S15	CSI0_D1- / PCAM_D15					Not used
S16	GND				P	Ground
S17	AFB0_OUT					SMSC LAN8720A Center tap reference voltage for GBE1 Carrier board Ethernet magnetic

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S18	AFB1_OUT	B6		AIN0	AI	XP: Plus X-axis on-off control signal
S19	AFB2_OUT	B7		AIN2	AI	YP: Plus Y-axis on-off control signal
S20	AFB3_IN					Not used
S21	AFB4_IN	C7		AIN1	AI	XM: Minus X-axis on-off control signal
S22	AFB5_IN	A7		AIN3	AI	YM: Minus Y-axis on-off control signal
S23	AFB6_PTIO				O OD	SMSC LAN8720A and OD driver GBE_1_ LINK100#: Link Speed Indication LED for 100Mbps for AFB 2nd GBE
S24	AFB7_PTIO					GBE_1_LINK1000#: Not used
S25	GND				P	Ground
S26	SDMMC_D0					Not used
S27	SDMMC_D1					Not used
S28	SDMMC_D2					Not used
S29	SDMMC_D3					Not used
S30	SDMMC_D4					Not used
S31	SDMMC_D5					Not used
S32	SDMMC_D6					Not used
S33	SDMMC_D7					Not used
S34	GND					Not used

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S35	SDMMC_CK					Not used
S36	SDMMC_CMD					Not used
S37	SDMMC_RST#					Not used
S38	AUDIO_MCK	D14	Mode0	XDMA_EVENT_INTR1	O	Master clock output to Audio codecs
S39	I2S0_LRCK	C13	Mode3	MCASP1_FSX	IO	Left& Right audio synchronization clock
S40	I2S0_SDOUT	D13	Mode3	MCASP1_AXR0	O	Digital audio Output
S41	I2S0_SDIN	A14	Mode3	MCASP1_AXR1	I	Digital audio Input
S42	I2S0_CK	B12	Mode3	MCASP1_ACLKX	IO	Digital audio clock
S43	I2S1_LRCK					Not used
S44	I2S1_SDOUT					Not used
S45	I2S1_SDIN					Not used
S46	I2S1_CK					Not used
S47	GND				G	Ground
S48	I2C_GP_CK	D15	Mode3	I2C1_SCL	IO OD	General purpose I2C bus clock
S49	I2C_GP_DAT	D16	Mode3	I2C1_SDA	IO OD	General purpose I2C bus data
S50	I2S2_LRCK					Not used
S51	I2S2_SDOUT					Not used
S52	I2S2_SDIN					Not used
S53	I2S2_CK					Not used
S54	SATA_ACT#					Not used

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S55	AFB8_PTIO				O OD	SMSC LAN8720A and OD driver GBE1_LINK_ACT# : Link / Activity Indication LED for AFB 2nd GBE Driven low on Link (10, 100 or 1000 mbps) Blinks on Activity,
S56	AFB9_PTIO					Not used
S57	PCAM_ON_CSI0#					Not used
S58	PCAM_ON_CSI1#					Not used
S59	SPDIF_OUT					Not used
S60	SPDIF_IN					Not used
S61	GND				P	Ground
S62	AFB_DIFF0+				AIO	GBE1_MDI0+: Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface) for AFB 2nd GBE, SMSC LAN8720A: Differential Transmit/Receive Positive Channel 0

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S63	AFB_DIFF0-				AIO	GBE1_MDI0-: Bi-directional transmit/receive pair 0 to magnetics (Media Dependent Interface) for AFB 2nd GBE, SMSC LAN8720A: Differential Transmit/Receive Negative Channel 0
S64	GND					
S65	AFB_DIFF1+				IO	GBE1_MDI1+: Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface) for AFB 2nd GBE, SMSC LAN8720A: Differential Transmit/Receive Positive Channel 1
S66	AFB_DIFF1-					GBE1_MDI1-: Bi-directional transmit/receive pair 1 to magnetics (Media Dependent Interface) for AFB 2nd GBE, SMSC LAN8720A: Differential Transmit/Receive Negative Channel 1
S67	GND				P	Ground
S68	AFB_DIFF2+					GBE1_MDI2+: Not used

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S69	AFB_DIFF2-					GBE1_MDI2-: Not used
S70	GND				P	Ground
S71	AFB_DIFF3+					GBE1_MDI3+: Not used
S72	AFB_DIFF3-					GBE1_MDI3-: Not used
S73	GND				P	Ground
S74	AFB_DIFF4+					Not used
S75	AFB_DIFF4-					Not used
S76	PCIE_B_RST#					Not used
S77	PCIE_C_RST#					Not used
S78	PCIE_C_RX+					Not used
S79	PCIE_C_RX-					Not used
S80	GND				P	Ground
S81	PCIE_C_TX+					Not used
S82	PCIE_C_TX-					Not used
S83	GND				P	Ground
S84	PCIE_B_REFCK+					Not used
S85	PCIE_B_REFCK-					Not used
S86	GND				P	Ground
S87	PCIE_B_RX+					Not used
S88	PCIE_B_RX-					Not used
S89	GND				P	Ground
S90	PCIE_B_TX+					Not used

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S91	PCIE_B_TX-					Not used
S92	GND				P	Ground
S93	LCD_D0	U10	Mode1	LCD_DATA23	O	8 bit BLU color data - 18 bit display implementations leave the two LS bits (D0, D1) not connected
S94	LCD_D1	U12	Mode1	LCD_DATA20	O	
S95	LCD_D2	V13	Mode0	LCD_DATA17	O	
S96	LCD_D3	U4	Mode0	LCD_DATA11	O	
S97	LCD_D4	V2	Mode0	LCD_DATA12	O	
S98	LCD_D5	V3	Mode0	LCD_DATA13	O	
S99	LCD_D6	V4	Mode0	LCD_DATA14	O	
S100	LCD_D7	T5	Mode0	LCD_DATA15	O	
S101	GND				P	Ground
S102	LCD_D8	T10	Mode1	LCD_DATA22	O	8 bit GRN color data - 18 bit display implementations leave the two LS bits (D8, D9) not connected
S103	LCD_D9	T12	Mode1	LCD_DATA19	O	
S104	LCD_D10	T2	Mode0	LCD_DATA5	O	
S105	LCD_D11	T3	Mode0	LCD_DATA6	O	
S106	LCD_D12	T4	Mode0	LCD_DATA7	O	
S107	LCD_D13	U1	Mode0	LCD_DATA8	O	
S108	LCD_D14	U2	Mode0	LCD_DATA9	O	
S109	LCD_D15	U3	Mode0	LCD_DATA10	O	
S110	GND				P	Ground

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S111	LCD_D16	T11	Mode1	LCD_DATA21	O	8 bit RED color data - 18 bit display implementations leave the two LS bits (D16, D17) not connected
S112	LCD_D17	R12	Mode1	LCD_DATA18	O	
S113	LCD_D18	U13	Mode1	LCD_DATA16	O	
S114	LCD_D19	R1	Mode0	LCD_DATA0	O	
S115	LCD_D20	R2	Mode0	LCD_DATA1	O	
S116	LCD_D21	R3	Mode0	LCD_DATA2	O	
S117	LCD_D22	R4	Mode0	LCD_DATA3	O	
S118	LCD_D23	T1	Mode0	LCD_DATA4	O	
S119	GND				P	Ground
S120	LCD_DE	R6	Mode0	LCD_AC_BIAS_EN	O	Display Enable- signal is high during the active display line; low otherwise
S121	LCD_VS	U5	Mode0	LCD_VSYNC	O	Vertical Sync- high pulse indicates the start of a new display frame
S122	LCD_HS	R5	Mode0	LCD_HSYNC	O	Horizontal Sync - high pulse indicates the start of a new horizontal display line
S123	LCD_PCK	V5	Mode0	LCD_PCLK	O	Pixel clock - display data transitions on the positive clock edge
S124	GND				P	Ground
S125	LVDS0+					Not used
S126	LVDS0-					Not used

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S127	LCD_BKLT_EN	U15	Mode7	GPIO1[22]	O	
S128	LVDS1+					Not used
S129	LVDS1-					Not used
S130	GND				P	Ground
S131	LVDS2+					Not used
S132	LVDS2-					Not used
S133	LCD_VDD_EN	T15	Mode7	GPIO1[23]	O	
S134	LVDS_CK+					Not used
S135	LVDS_CK-					Not used
S136	GND				P	Ground
S137	LVDS3+					Not used
S138	LVDS3-					Not used
S139	I2C_LCD_CK	D17	Mode3	I2C2_SCL	O OD	LCD display I2C bus clock
S140	I2C_LCD_DAT	D18	Mode3	I2C2_SDA	IO OD	LCD display I2C bus data
S141	LCD_BKLT_PWM	T6	Mode2	TIMER5	O	Display backlight PWM control
S142	LCD_DUAL_PCK					Not used
S143	GND				P	Ground
S144	RSVD / EDP_HPD					Not used
S145	WDT_TIME_OUT#	R7	Mode2	TIMER4	O	Watchdog-Timer Output
S146	PCIE_WAKE#					Not used

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S147	VDD_RTC				P	Low current RTC circuit backup power - 3.0V nominal It is sourced from a Carrier based Lithium cell or Super Cap
S148	LID#					Reserved(1)
S149	SLEEP#					Reserved(1)
S150	VIN_PWR_BAD#				I	PMIC TPS65217C, Power bad indication from Carrier board. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) will not be enabled while this signal is held low by the Carrier. Pulled up on Module. Driven by OD part on Carrier.
S151	CHARGING#					Reserved(1)
S152	CHARGER_PRSNT#					Reserved(1)
S153	CARRIER_STBY#					Reserved(1)

SMARC Edge Finger		Sitara AM335x CPU			Type	Description
Pin#	Pin Name	Ball	Mode	Signal Name		
S154	CARRIER_PWR_ON				O	PMIC TPS65217C, Carrier board circuits (apart from power management and power path circuits) will not be powered up until the Module asserts the CARRIER_PWR_ ON signal.
S155	FORCE_RECOV#					Not used
S156	BATLOW#					Reserved
S157	TEST#					Not used
S158	VDD_IO_SEL#				IO	Tied to high to indicate 3.3V I/O on module

Note: Due to the insufficient IO pin number of Sitara AM335x, the reserved pins are multiplexed with RMII2 related pins and default will be configured as RMII2.

Handshaking between SMARC Module and Carrier

This Chapter points out the handshaking rule between SMARC module and carrier.
Section include：

- SMARC T335X Module Power
- Terminations
- Boot Select

Chapter 4 Handshaking between SMARC T335x Module and Carrier

SMARC module has specific handshaking rules to the carrier by SMARC hardware specification. To design the carrier board, users need to follow these rules or it might not boot up. Some pull-up and pull-down also need to be cared to make all functions work.

4.1 SMARC T335x Module Power

4.1.1. Input Voltage / Main Power Rail

The allowable Module DC input voltage range for T335x is from 3.35V to 5.25V. This voltage is brought in on the VDD_IN pins and returned through the numerous GND pins on the connector. The SMARC specification defines the input voltage range should extend down to 3.0V. The SMARC T335X lower limit is determined by a non-volatile register setting in the TI PMIC used and is set 3.35V by default. A single 5V DC input is recommended.

Ten pins are allocated to VDD_IN. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins. At the lowest allowed Module input voltage, this would allow up to 16.75W of electrical power to be brought in (with no de-rating on the connector current capability). With a 40% connector current de-rating, up to 10W may be brought in at 3.35V.
T335x typically consumes 1.5W and is pretty safe in using the connector.

4.1.2. No Separate Standby Voltage

There is no separate voltage rail for standby power, other than the very low current RTC voltage rail. SMARC T335x operating and standby power comes from the single set of VDD_IN pins. This suits battery power sources well, and is also easy to use with non-battery sources.

4.1.3. RTC/Backup Voltage

RTC backup power is brought in on the VDD_RTC rail. The RTC consumption is typically 15 microA or less. The allowable VDD_RTC voltage range shall be 2.0V to 3.25V. The VDD_RTC rail is sourced from a Carrier based Lithium cell, or it may be left open if the RTC backup functions are not required. SMARC T335x module is able to boot without a VDD_RTC voltage source.

Lithium cells, if used on Carrier, shall be protected against charging by a Carrier Schottky diode. The diode is placed in series with the positive battery terminal. The diode anode is on the battery side, and the cathode on the Module VDD_RTC side.

Note that if a Super cap is used, current may flow out of the Module VDD_RTC rail to charge the Super Cap.

4.1.4. Power Sequencing

The Module signal *CARRIER_PWR_ON* exists to ensure that the Module is powered before the main body of Carrier circuits (those outside the power and power control path on the Carrier). The main body of Carrier board circuits should not be powered until the Module asserts the *CARRIER_PWR_ON* signal as a high. Module hardware will assert *CARRIER_PWR_ON* when all Module supplies necessary for Module booting are up.

4.1.5. VDD_IO

The default I/O voltage for SMARC T335x module is 3.3V only. SMARC specification defines the I/O voltage to be 1.8V or 3.3V or both.

Due to SMARC T335x supports only 3.3V I/O, it pull the *VDD_IO_SEL#* pin to the Module *VDD_IN* rail through a resistance of 100K as defined in SMARC specification. If the Carrier supports only 1.8V I/O, then the Carrier will tie the *VDD_IO_SEL#* pin directly to GND. If the Carrier supports only 3.3V like the case here, Carriers will float the signal for 3.3V.
SMARC T335x will not power up if T335x senses a 1.8V *VDD_IO* Carrier on the *VDD_IO_SEL#* (due to the Carrier pulling the line down) and the Module supports only 3.3V I/O.

4.1.6. Power Bad Indication (VIN_PWR_BAD#)

Power bad indication is from carrier board and is an input signal for Module. Module and Carrier power supplies (other than Module and Carrier power supervisory circuits) will not be enabled while this signal is held low by the Carrier.
This signal has a 100K pull-up on module and is driven by OD part on Carrier.

4.1.7. System Power Domains

It is useful to describe an SMARC system as being divided into a hierarchy of three power domains:
1) Battery Charger power domain (can be neglected if the system is not battery powered only)
2) SMARC Module power domain
3) Carrier Circuits power domain
The Battery Charger domain includes circuits that are active whenever either charger input power and / or battery power are available. These circuits may include power supply supervisor(s), battery chargers, fuel gauges and, depending on the battery configuration, switching power section(s) to step down a high incoming battery voltage.
The SMARC Module domain includes the SMARC module.
The Carrier Circuits domain includes “everything else” (and does not include items from the Battery Charger and Module domain, even though they may be mounted on the Carrier).
This is illustrated in the figure below.

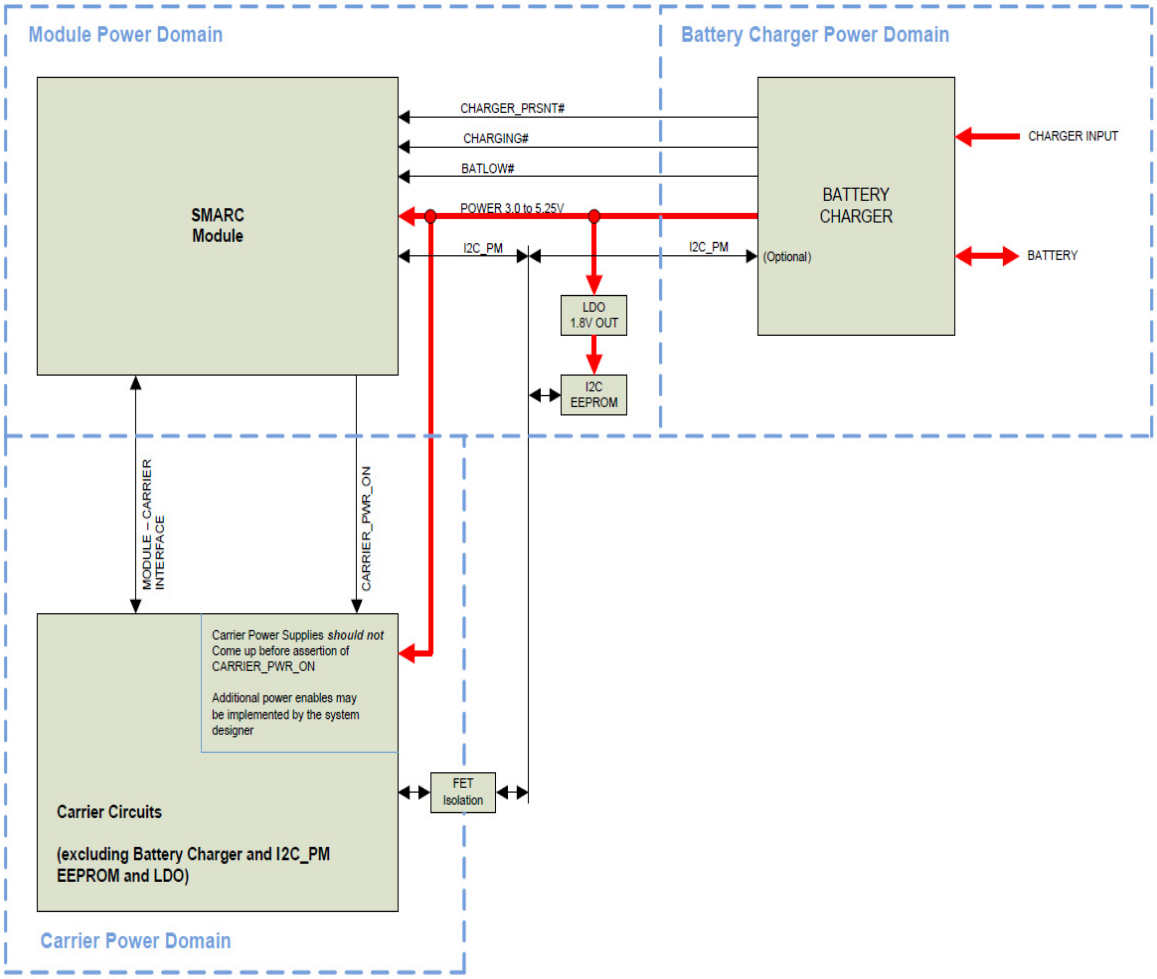


Figure 16 System Power Domains

4.2 Terminations

4.2.1. Module Terminations

The Module signals listed below will be terminated on the Module. The terminations follow the guidance given in the table below.

Signal Name	Series Termination	Parallel Termination	Notes
I2C_PM_DAT		2.2K pull-up to 1.8V	
I2C_PM_CK		2.2K pull-up to 1.8V	
I2C_LCD_DAT		2.2K pull-up to VDD_IO	
I2C_LCD_CK		2.2K pull-up to VDD_IO	
I2C_CAM_DAT		2.2K pull-up to VDD_IO	
I2C_CAM_CK		2.2K pull-up to VDD_IO	
I2C_GP_DAT		2.2K pull-up to VDD_IO	
I2C_GP_CK		2.2K pull-up to VDD_IO	
USBx_EN_OC#		10K pull-up to 3.3V	x is '0' '1' or '2' Switched 3.3V
USB0_OTG_ID		10K pull-up to 3.3V	
VDD_IO_SEL#		100k pull-up to VIN	
VIN_PWR_BAD#		100k pull-up to VIN	
TXP (pin 21 of LAN8720A)		49.9ohm, 1.0% pull-up resistor to VDDA (created from +3.3V through a ferrite bead)	
TXN (pin 22 of LAN8720A)		49.9ohm, 1.0% pull-up resistor to VDDA	

Signal Name	Series Termination	Parallel Termination	Notes
RXP (pin 23 of LAN8720A)		49.9ohm, 1.0% pull-up resistor to VDDA	
RXN (pin 22 of LAN 8720A)		49.9ohm, 1.0% pull-up resistor to VDDA	
LED1/REGOFF (pin 3)		10kohm, 1.0% pull-down resistor to ground.	
LED2/nINTSEL (pin 2)		10kohm,1.0% pull-down resistor to ground	
All other Module inputs		Weak (~47K) termination to inactive state	

4.2.2. Carrier/Off-Module Terminations

The following Carrier terminations are required, if the relevant interface is used. If unused, the SMARC Module pins may be left un-connected.

Module Signal Group Name	Carrier Series Termination	Carrier Parallel Termination	Notes
GBE_MDI	Magnetics module appropriate for 10/100/1000 GBE transceivers	Secondary side center tap terminations appropriate for Gigabit Ethernet implementations	
GBE_LINK (GBE status LED sinks)		If used, current limiting resistors and diodes to pulled to a positive supply rail	The open drain GBE status signals, GBE_LINK100#, GBE_LINK1000# and GBE_LINK_ACT#, if used, need Carrier based current limiting resistors and LEDs. The LED may be integrated into a Carrier RJ45 jack. A resistor of 68 ohms, and a LED with the anode tied to Carrier 3.3V, is typical.
LVDS LCD		100 ohm resistive termination across the differential pairs at the endpoint of the signal path, usually on the display assembly	

4.3 Boot Device Selection

SMARC hardware specification defines three pins (*BOOT_SEL[0:2]*) that allow the Carrier board user to select from eight possible boot devices. Sitara AM335x bases on *SYSBOOT* configuration to determine the boot devices. The boot select utilizes *SYSBOOT* and line decoder/de-multiplexer logic to meet the SMARC specification. The *BOOT_SELx#* pins are weakly pulled up on the Module and the pin states decoded by module logic. The Carrier shall either leave the Module pin Not Connected ("Float" in the table below) or shall pull the pin to GND, per the table below.

	Carrier Connection			Boot Source
	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
0	GND	GND	Float	Carrier SD Card
1	Float	Float	GND	Module eMMC Flash
2	GND	Float	Float	Carrier SPI